

# Module Catalog

*M.Sc. Microelectronics and Chip Design*

Degree Program M.Sc. Microelectronics and Chip Design

Technische Universität München

[www.tum.de/](http://www.tum.de/)

## Module Catalog: General Information and Notes to the Reader

### **What is the module catalog?**

One of the central components of the Bologna Process consists in the modularization of university curricula, that is, the transition of universities away from earlier seminar/lecture systems to a modular system in which thematically-related courses are bundled together into blocks, or modules.

This module catalog contains descriptions of all modules offered in the course of study.

Serving the goal of transparency in higher education, it provides students, potential students and other internal and external parties with information on the content of individual modules, the goals of academic qualification targeted in each module, as well as their qualitative and quantitative requirements.

### **Notes to the reader:**

#### **Updated Information**

An updated module catalog reflecting the current status of module contents and requirements is published every semester. The date on which the module catalog was generated in TUMonline is printed in the footer.

#### **Non-binding Information**

Module descriptions serve to increase transparency and improve student orientation with respect to course offerings. They are not legally-binding. Individual modifications of described contents may occur in praxis.

Legally-binding information on all questions concerning the study program and examinations can be found in the subject-specific academic and examination regulations (FPSO) of individual programs, as well as in the general academic and examination regulations of TUM (APSO).

#### **Elective modules**

Please note that generally not all elective modules offered within the study program are listed in the module catalog.

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## Master's Thesis | Masterarbeit

### Module Description

#### EI8950: Master's Thesis | Masterarbeit

Version of module description: Gültig ab winterterm 2025/26

<b>Module Level:</b> Master	<b>Language:</b> German/English	<b>Duration:</b> one semester	<b>Frequency:</b> winter/summer semester
<b>Credits:*</b> 30	<b>Total Hours:</b> 900	<b>Self-study Hours:</b> 900	<b>Contact Hours:</b> 0

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The module examination consists of the following parts:

- Scientific write-up of the Master's Thesis (ca. 50 - 100 pages): The student proves ability to individually solve a problem within the field of the Master' Degree by creating individual concepts and conducting hands-on research (100% of module grade).
- Final presentation (ca. 20 minutes): With the final presentation the student proves the ability to present, reflect, and discuss methods and results in a structured way.

The language of the module examination (German/English) depends on the specifications in the study regulations (FPSO) of the respective degree program.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Permit of the board of examiners, proofing a sufficient study progress according to the exam regulations

#### Content:

Every student self-responsibly works with scientific methods on an individual research topic as agreed with the scientific examiner that deals with a problem within the field of the Master's Degree.

#### Intended Learning Outcomes:

After successful completion of the module, students are able to define a scientific problem within the field of the Master's Degree or categorize a problem within existing theories. They are able to identify, discuss, and apply suitable methods to the problem out of the methods learned during

studies as well as relevant literature. The abilities include discussion and presentation of results with both supervisor and interested audience, drawing conclusions, and setting and following a timeline or project plan within the given deadlines.

**Teaching and Learning Methods:**

During the participation in the module the students practice engineering. The Master's Thesis has the format of a project work that not only contains manual task, but also planning and conceptual elements that are part of the work scope in professional engineering life.

Every participant works on an individual technical task, especially in independent way.

Every participant is assigned a scientific advisor matching the topic. The advisor assists especially during the early stage of the work, presenting the technical background of the topic, preparing relevant literature and by giving helpful hints both during the technical work and during the creation of the written documentation and presentation.

**Media:**

Self-study / practical work under the guidance of a scientific examiner

**Reading List:**

J Michael Bennett, Project Management for Engineers, 2014

**Responsible for Module:**

Studiendekan / Dean of Academic Affairs

**Courses (Type of course, Weekly hours per semester), Instructor:**

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Examination Performance | Prüfungsleistungen

### Fundamental Laboratory Courses | Grundlagenpraktikum

#### Module Description

### CIT431016: HDL Chip Design Laboratory | HDL Chip Design Laboratory [HDLCDL]

Version of module description: Gültig ab winterterm 2024/25

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter/summer semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 90	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The achievement of the module's learning outcomes is assessed through practical exercises consisting of four programming tasks. Additionally, students have the opportunity to participate in an optional midterm exam.

#### Programming Tasks:

Through the programming tasks, students demonstrate their ability to design and develop an embedded system on FPGA. For this purpose, students write HDL code for a given system, perform simulations of the system, test their system on an FPGA, debug their code, and document the components they have developed.

#### Optional Midterm Exam (graded written exam, 60 minutes):

In the exam, students demonstrate their ability to understand design concepts for integrated and embedded systems, as well as to analyze and evaluate these systems by answering questions. Tasks may include interpreting results from a design simulation or theoretical questions about the concept of an embedded system.

The final grade is based 100% on the programming tasks. An improvement through the midterm exam is possible. In this scenario, the final grade is calculated based on a combination of "75% programming task grade" and "25% midterm grade," as long as the student achieves a passing grade of at least 4.0 in the programming tasks and the weighting results in an overall grade improvement.

**Repeat Examination:**

Next semester

**(Recommended) Prerequisites:**

Fundamentals of digital logic design

Fundamentals of programming

**Content:**

Concept of an integrated electronic system; build an example of an integrated system with a microcontroller, bus, and peripherals; first implement an encryption algorithm using a standard hardware description language; then wrap the security module as a peripheral attached to the bus; design an interface between peripheral and bus; apply an FPGA design flow for embedded systems, and embedded software for testing the encryption algorithm.

**Intended Learning Outcomes:**

By the end of the module, students will be able to analyze and evaluate concepts of integrated and embedded systems (“chips”). They will be capable of designing and creating integrated and embedded systems (particularly an embedded system with FPGA, bus, and peripherals) with their complex system components using a standardized hardware description language (HDL) and an FPGA design flow.

**Teaching and Learning Methods:**

Learning method:

In addition to the students' individual methods, consolidated knowledge is acquired by providing subtasks of increasing complexity and difficulty in the laboratory notes.

Teaching method:

Students are free to work on the laboratory tasks independently, according to their schedule.

Students can work in the laboratory either in institute rooms or at home. An adviser is available to support them in case of significant difficulties.

**Media:**

The following kinds of media are used:

- \* Introductory lectures
- \* Lecture slides available
- \* Laboratory notes with detailed descriptions of tasks and tool environments
- \* Individual discussions with advisor

**Reading List:**

The following literature is recommended:

\* ANSI, IEEE Standards Board, IEEE Standard VHDL Language Reference Manual: IEEE Std 1076-1993 , New York, 1988, ISBN 1559373768

\* Peter J. Ashenden, Designer s Guide to Vhdl, Morgan Kaufmann Publishers, 1995, ISBN 1558602704

\* More literature listed in laboratory notes

**Responsible for Module:**

Schlichtmann, Ulf; Prof. Dr.-Ing.

**Courses (Type of course, Weekly hours per semester), Instructor:**

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### CIT441019: Lab Analog Chip Design | Lab Analog Chip Design [Lab ACD]

*Laboratory Course Analog Chip Design*

Version of module description: Gültig ab winterterm 2025/26

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 90	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The examination is completed in the form of a project. This consists of a project assignment with a practical project part that demonstrates a basic understanding of the practical side of developing an integrated analog circuit, the ability to dimension the transistors it contains in a design tool, the ability to optimize such a circuit and an understanding of the interaction between the design tool and PDK. The project part is worked on by the students in small groups of approx. two students. The individual contribution to the individual work steps in the project part is documented in writing by the students (the scope of the documentation is 2 to 5 pages per student). The ability to justify and defend their own design decisions on the basis of the basic understanding they have acquired and to present them in an illustrated manner, summarized to the essential core and communicate them to a knowledgeable audience is demonstrated in a group presentation (10 minutes per student, i.e. 20 minutes for a group of two) followed by questions. The documentation (25% of the overall grade) and the presentation (75% of the overall grade) are used for the individual grading of the internship.

#### Repeat Examination:

End of Semester

#### (Recommended) Prerequisites:

Basic knowledge of circuit design and MOSFET operation

#### Content:

The students will learn the basics of analog integrated circuit design using Cadence Virtuoso. This includes:

- MOSFET operation and biasing
- Simple Amplifier Circuits
- Basic and advanced Current Mirrors

- OTA design and amplifier metrics
- Miller OpAmp
- Advanced OTA configurations and design

The students will gain hands-on experience in designing integrated circuits with state of the art EDA software and gain a basic knowledge of analog design techniques.

**Intended Learning Outcomes:**

After successfully completing the lab, the students have a basic understanding of the design of analog integrated circuits. They are able to explain to analyze science-based their design decisions of analog integrated circuits and critically reflect on them. They can bias a transistor according to its function in an analog circuit and are able to optimize their behavior. Additionally, they are able to use the basic functionalities of Cadence Virtuoso and know the connections between tooling and PDK. Students can illustrate using suitable media and summarize the steps involved in the development of an integrated analog circuit and communicate them competently.

**Teaching and Learning Methods:**

Independent simulation according to course instructions under supervision. Own presentation at the end of the course.

Five guided practical experiments with theory discussion and practical simulation of circuits and circuit concepts with Cadence Virtuoso. The simulations are carried out in groups of two or three with on-site supervision. After each experiment there will be a discussion and explanation with the supervisor.

**Media:**

Course script, Simulation software

**Reading List:**

W. Sansen: Analog Design Essentials  
J. Baker: CMOS Circuit Design, Layout and Simulation  
B. Razavi: Design on Analog CMOS Integrated Circuits

**Responsible for Module:**

Stefan Pechmann: stefan.pechmann@tum.de; Prof. Dr.-Ing. Amelie Hagelauer:  
amelie.hagelauer@tum.de

**Courses (Type of course, Weekly hours per semester), Instructor:**

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Scientific Seminar | wissenschaftliches Seminar

### Module Description

#### CIT4320000: Seminar on Topics in Design Automation | Seminar on Topics in Design Automation [Seminar CDA] *Seminar on Topics in Design Automation*

Version of module description: Gültig ab winterterm 2022/23

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter/summer semester
<b>Credits:*</b> 5	<b>Total Hours:</b>	<b>Self-study Hours:</b> 105	<b>Contact Hours:</b> 45

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

During the semester, the students study a chosen topic and prepare a corresponding presentation. The resulting presentation (about 20 minutes with a following 10 minute discussion) determines 70% of the final grade. Afterwards, the students prepare a written report regarding the chosen topic (and also including possible feedback from the presentation) which determines 30% of the final grade.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

No specific requirements

#### Content:

In this seminar, current topics from the area of Design Automation are discussed among the participants. A structured introduction into scientific literature regarding paper reading, literature research, presentation techniques, and scientific writing is given. The participants are enabled to independently perform all required steps to present a scientific topic in form of a review paper and an oral presentation.

#### Intended Learning Outcomes:

Upon successful completion of the module, the participants are able to investigate a scientific topic based on the reading and further research of scientific publications in the area of Design Automation. The participants are able to critically reflect and discuss research outcomes. They are

able to structure and write a scientific report. The participants are able to present the contents of their findings and participate in a scientific discussion.

**Teaching and Learning Methods:**

Each student independently works on the chosen topic. A kick-off meeting provides information and resources regarding the scientific research and writing methods as well as the form of the final oral presentation. Additionally, each participant has a personal supervisor. This supervisor should help at the beginning of the research by providing according literature as well as definition and focus of the topic. The supervisor helps the students with questions and scientific discussions.

**Media:**

- Presentation
- Report
- Discussions

**Reading List:**

**Responsible for Module:**

Wille, Robert; Prof. Dr.-Ing.

**Courses (Type of course, Weekly hours per semester), Instructor:**

Seminar on Topics in Design Automation (Seminar, 3 SWS)

Wille R [L], Wille R

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### CIT4320002: Seminar AI Processor Design | Seminar AI Processor Design [AIPro-seminar]

Version of module description: Gültig ab winterterm 2023/24

<b>Module Level:</b> Bachelor/Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter/summer semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 90	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The examination is based on a scientific elaboration. This examination consists of a written part (50%) in form of a paper (4 pages), and of an oral part (50%) in form a presentation of approximately 30 minutes (including a subsequent discussion and questions). Through the scientific elaboration students show that they can prepare, structure and present, e.g., the state-of-the-art, new ideas or existing approaches on novel computing concepts that employ non-traditional methods to accelerate Artificial Intelligent (AI) workloads.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

None.

#### Content:

Technology scaling is approaching its end in which breakthroughs become inevitable. This holds even more after starting the massive production of commercial processors at 7nm technology nodes. At such an extreme scale, obtaining further improvements in the efficiency of processors become significantly difficult. AI applications, in practical, impose profound challenges for the exiting von-Neumann architectures.

Specific seminar topics in the area of AI acceleration in both hardware and software will be offered.

Examples are:

\* In-memory and near-memory computing to largely accelerate AI applications.

- \* Lightweight deep learning algorithms for edge AI such as quantized neural networks (QNNs) and binarized neural networks (BNNs).
- \* Brain-inspired computing hardware such as neuromorphic computing and spiking neural networks (SNNs).
- \* Emerging non-volatile memories and their crucial role in mimicking biological computing systems (e.g., membrane and synapses).
- \* Emerging technologies for future ultralow power AI processors.
- \* Brain-inspired computing algorithms such as novel hyperdimensional computing.

### **Intended Learning Outcomes:**

At the end of the seminar, the students are able to present a new idea or an existing approach in the area of AI acceleration in an understandable and convincing manner.

For this purpose, the following competencies will be acquired:

- \* The students are able to independently familiarize themselves with a scientific topic in the field of unconventional computing paradigms for AI accelerations.
- \* The students are able to present their topic in a structured way according to problem formulation, state of the art, goals, methods and results.
- \* The students can present their topic, according to the above-mentioned structure, in form of a presentation, and in form of a written report.

The students are able to summarize, present, and explain research ideas presented in scientific papers.

### **Teaching and Learning Methods:**

Learning method:

Students elaborate a given scientific topic by themselves and are advised by a research assistant.

Teaching method:

Introductory lessons will be given, which cover advice on the work procedure during the seminar, scientific writing techniques as well as the preparation of an oral presentation.

The students discuss further (specific) details with the advising research assistants on an individual basis.

### **Media:**

All current techniques for preparing and presenting papers and talks will be applied, e.g.

- blackboard, whiteboard
- electronic slides, beamer
- electronic word processing
- electronic slide processing

### **Reading List:**

David Harris and Sarah Harris, Digital Design and Computer Architecture (Second Edition), August 2012, Morgan Kaufmann Publishers, San Francisco, CA, United States

Charu C. Aggarwal, Artificial Intelligence: A Textbook, July 2022, Springer International Publishing, Basel, Switzerland

A set of topics and related literature is given at the start of the course. Each participant selects his/her topic.

**Responsible for Module:**

Amrouch, Hussam; Prof. Dr.-Ing.

**Courses (Type of course, Weekly hours per semester), Instructor:**

Seminar AI Processor Design (Seminar, 4 SWS)

Amrouch H, Dhakad N, Genßler P, Thomann S

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### CIT442005: Seminar Analog Chip Design | Seminar Analog Chip Design [Sem ACD]

#### *Seminar Analog Chip Design*

Version of module description: Gültig ab winterterm 2024/25

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter/summer semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 105	<b>Contact Hours:</b> 45

Number of credits may vary according to degree program. Please see Transcript of Records.

#### **Description of Examination Method:**

During the Semester, the students will write a scientific report of 3-4 pages about a topic provided by a supervisor in form of a scientific publication. The report will be 75% of the overall grade.

Each participant will hold a final presentation (20 Min) with a 10 minutes discussion after the presentation. The presentation will determine 25% of the overall grade.

With the scientific report, the participants of the seminar show that they can implement and apply standards for scientific publications, such as correct citation or independent familiarization with scientific literature. This will be assessed by the supervisor on the basis of the paper. With the presentation it is assessed whether students can present their correct content with scientifically correct technical language, clear explanations of the topic and appropriate answers to questions during the discussion.

#### **Repeat Examination:**

Next semester

#### **(Recommended) Prerequisites:**

None

#### **Content:**

Changing topics in the overall field of analog, integrated circuit design, which are provided and supervised by members of the chair. The participants are researching the topic on their own and write a scientific paper with supervision of a PhD student. A Kick-Off meeting as well as a final presentation conclude the seminar.

**Intended Learning Outcomes:**

After doing the seminar, the students will be able to do research regarding a scientific topic using resources provided by the scientific community (papers, journals, books). The students are able to write a publication which fulfills the formal requirements of a scientific paper in the IEEE style. Additionally, the students will present the researched topic in a university environment.

**Teaching and Learning Methods:**

Presentation of the researched topic as well as writing a paper about it with clear requirements, which meet the standard of an IEEE publication.

**Media:**

presentation  
scientific paper template

**Reading List:**

IEEE Xplore  
Google Scholar  
Example Paper:  
Pechmann, S.; Mai, T.; Völkel, M.; Mahadevaiah, M.K.; Perez, E.; Perez-Bosch Quesada, E.; Reichenbach, M.; Wenger, C.; Hagelauer, A. A Versatile, Voltage-Pulse Based Read and Programming Circuit for Multi-Level RRAM Cells. Electronics 2021, 10, 530. <https://doi.org/10.3390/electronics10050530>

**Responsible for Module:**

Stefan Pechmann: [stefan.pechmann@tum.de](mailto:stefan.pechmann@tum.de); Prof. Dr.-Ing. Amelie Hagelauer: [amelie.hagelauer@tum.de](mailto:amelie.hagelauer@tum.de)

**Courses (Type of course, Weekly hours per semester), Instructor:**

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### EI5092: Seminar on Security in Information Technology | Seminar on Security in Information Technology

Version of module description: Gültig ab winterterm 2025/26

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 105	<b>Contact Hours:</b> 45

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The examination takes the form of a scientific paper. On the one hand, it consists of a written part (50%), which consists of a paper (4 pages) with which students demonstrate their ability to prepare a research topic in writing. On the other hand, it consists of an oral part (50%) in the form of an approx. 30-minute presentation (including subsequent discussion). With this, students demonstrate that they are able to prepare scientific content for a specialist audience and present it in a suitable form.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

The following modules should be passed before selecting this module:

- Kryptologie or similar base-level course

Additionally, the following courses are recommended:

- Sichere Implementierung kryptographischer Verfahren
- Selected Topics in System Security

#### Content:

Topics on security of systems for information technology with varying focus:

Students of this modul work independently on current scientific topics and write a scientific report. Finally, a presentation of the results of the work is given to all module participants. The understanding of the topic is deepened by intensive discussion.

**Intended Learning Outcomes:**

After successful completion of the module, students have knowledge on current problems and hot topics in the field of security of systems for information technology.

Afterwards, the students is capable to carry out scientific work on up-to-date topics in the field of security of systems for information technology, to write scientific papers, and to asses the value of scientific papers. Furthermore, students are able to present the acquired knowledge to a scientific audience by a talk.

**Teaching and Learning Methods:**

An individual subject-specific task has to be solved by each participant autonomously.

With all tasks, a specific supervisor is associated who supports the participant. The support especially focuses on the beginning of the seminar where the supervisor helps the assigned participant to become acquainted with the topic and to find reasonable literature to start with. Supervisors will also provide hints to solve the task and to prepare the paper and the presentation.

Furthermore, a presentation training will be carried out and an introduction to scientific writing will be offered.

**Media:**

- Slides for presentations of the participants

**Reading List:**

- Oertner, Monika; St. John, Ilona; Thelen, Gabriele 2014: Wissenschaftlich schreiben. Ein Praxisbuch für Schreibtrainer und Studierende. Paderborn: Wilhelm Fink.

- Debdeep Mukhopadhyay, Rajat Subhra Chakraborty 2015; Hardware Security - Design, Threats, and Safeguards.CRC Press; ISBN: 978-1-4398-9583-2

**Responsible for Module:**

Sigl, Georg; Prof. Dr.-Ing.

**Courses (Type of course, Weekly hours per semester), Instructor:**

Seminar on Security in Information Technology (Hauptseminar, 3 SWS)

Pehl M ( Wettermann M )

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### EI77501: Seminar on Topics in Integrated Systems | Seminar on Topics in Integrated Systems [MSCE LIS Seminar]

Version of module description: Gültig ab winterterm 2022/23

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 105	<b>Contact Hours:</b> 45

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The examination is in a form of a scientific preparation that consists of a written part in form of a paper (typically 4 pages) and of a 20-minutes presentation followed by 5 minutes discussion. By the means of the exam students proof their ability to summarize and present e.g. the scientific state of the art, a new idea or an existing approach to integrated systems building blocks and architectures.

The grading consists of two elements:

- 50% written material
- 50% oral presentation and discussion

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

None.

#### Content:

Specific seminar topics in the area of electronic design automation will be offered. Examples are application-specific accelerators and function-specific processor architectures.

The participants independently work on a scientific topic, write a paper of typically 4 pages and present their topic in a talk. In the subsequent discussion the topic will be treated in-depth.

#### Intended Learning Outcomes:

At the end of the seminar, the students is able to present a state-of-the-art literature review in the area of integrated systems building blocks and architectures in an understandable and convincing manner.

The following competencies will be acquired:

- \* The student is able to independently analyze state-of-the-art concepts in the field of integrated systems.
- \* The student is able to present a topic in a structured way according to problem formulation, state of the art, goals, methods, and results.
- \* The student can present a topic according to the structure given above orally, with a set of slides, and with a written report.

### **Teaching and Learning Methods:**

Learning method:

Students elaborate a given scientific topic by themselves in coordination with the respective research assistant.

Teaching method:

Introductory lessons will be given by the course coordinator, further details are discussed between research assistant and student on an individual basis. Presentation skills will be taught in an introductory seminar.

### **Media:**

All current techniques for preparing and presenting papers and talks will be applied, e.g.

- blackboard, whiteboard
- electronic slides, beamer
- electronic word processing
- electronic slide processing

### **Reading List:**

- M. Hübner, J. Becker (Editors), "Multiprocessor System-on-Chip: Hardware Design and Tool Integration", Springer, 2010
- J. Teich, J. Henkel, A. Herkersdorf (Editors), "Invasive Computing", FAU University Press, 2022

A set of topics and related literature is given at the start of the course. Each participant selects his/her topic.

### **Responsible for Module:**

Herkersdorf, Andreas; Prof. Dr.

### **Courses (Type of course, Weekly hours per semester), Instructor:**

Seminar on Topics in Integrated Systems (Seminar, 3 SWS)

Wulff W [L], Herkersdorf A, Stechele W, Wild T, Twardzik T

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### EI77502: Seminar on Topics in Electronic Design Automation | Seminar on Topics in Electronic Design Automation [MSCE EDA Seminar]

Version of module description: Gültig ab winterterm 2022/23

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 105	<b>Contact Hours:</b> 45

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The examination is based on a scientific elaboration. This examination consist of a written part (50%) in form of a paper (4 pages), and of an oral part (50%) in form a presentation of approximately 30 minutes (including a subsequent discussion). Through the scientific elaboration students show that they can prepare, structure and present, e.g., the state-of-the-art, a new idea or an existing approach in the area of electronic design automation.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

None.

#### Content:

Specific seminar topics in the area of electronic design automation will be offered. Examples are analog design methodology, digital design methodology, layout synthesis, and system-level design methodology.

The students work independently on a scientific topic and write a paper of 4 pages. At the end of the seminar, the students present their topic during a scientific talk. In a subsequent discussion the topic will be treated in-depth.

#### Intended Learning Outcomes:

At the end of the seminar, the students are able to present a new idea or an existing approach in the area of computer-aided circuit and system design in an understandable and convincing manner.

For this purpose, the following competencies will be acquired:

- \* The students are able to independently familiarize themselves with a scientific topic in the field of electronic design automation
- \* The students are able to present their topic in a structured way according to problem formulation, state of the art, goals, methods and results.
- \* The students can present their topic, according to the above mentioned structure, in form of a presentation, and in form of a written report.

**Teaching and Learning Methods:**

Learning method:

Students elaborate a given scientific topic by themselves and are advised by a research assistant.

Teaching method:

Introductory lessons will be given, which cover advice on the work procedure during the seminar, scientific writing techniques as well as the preparation of an oral presentation.

The students discuss further (specific) details with the advising research assistants on an individual basis.

**Media:**

All current techniques for preparing and presenting papers and talks will be applied, e.g.

- blackboard, whiteboard
- electronic slides, beamer
- electronic word processing
- electronic slide processing

**Reading List:**

A set of topics and related literature is given at the start of the course. Each participant selects his/her topic.

**Responsible for Module:**

Schlichtmann, Ulf; Prof. Dr.-Ing.

**Courses (Type of course, Weekly hours per semester), Instructor:**

Seminar on Topics in Electronic Design Automation (Seminar, 3 SWS)

Foik C, Schlichtmann U

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### EI77503: Scientific Seminar on Structure, Architecture and Application of Sensor Circuits | Scientific Seminar on Structure, Architecture and Application of Sensor Circuits

Version of module description: Gültig ab summerterm 2021

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter/summer semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 105	<b>Contact Hours:</b> 45

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The academic performance consists of the preparation of a scientific article and a 15-minute presentation. This includes regular discussions with the assigned supervisor (research assistant) about the progress of the work and the procedure.

The module examination consists of the following components:

- Written elaboration of the results as a four-page scientific article.
- Elaboration and presentation of the results (15 minutes) with subsequent discussion / colloquium (5 min)

#### Repeat Examination:

#### (Recommended) Prerequisites:

Solid-State and Semiconductor Device Physics, Analog and Mixed-Signal Electronics

#### Content:

In this seminar the state of the art of application specific sensor systems and circuits shall be evaluated. Integrated circuit concepts and their application specific needs will be the core topic of the research.

The participants - in close contact to scientific staff members of the chair - will work out the state of the art in current scientific topics. A list of the topics offered for research will be published before the semester start on the homepage of the chair. In an introduction session at the beginning of the semester these topics will be assigned according to students interest.

Despite of the individual support of the scientific topics, two lectures to the soft skill topics of literature research, on how to write publications and on the art of a good presentation will be offered.

**Intended Learning Outcomes:**

After participating in the module event, students will be able to work on a circuit concept for specific applications in a scientific way, present the results to an expert audience and then engage in discussion of the results.

**Teaching and Learning Methods:**

**Media:**

**Reading List:**

Literature will be discussed during the first lecture and can be accessed via TUM library

**Responsible for Module:**

Brederlow, Ralf; Prof. Dr.-Ing.

**Courses (Type of course, Weekly hours per semester), Instructor:**

Scientific Seminar on structure, architecture, and application of sensor circuits (Seminar, 3 SWS)  
Brederlow R, Korek E, Verma V, Xu P, Chlan T, Riehm C, Schewa M, Ochs M, Ahrens H, Dietl M, David K

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Core Elective Modules | Kernbereiche

### Digital Design | Digital Design

#### Module Description

### CIT433032: Logic Synthesis and Physical Design | Logic Synthesis and Physical Design [Synthesis & Physical Design]

Version of module description: Gültig ab summerterm 2025

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> summer semester
<b>Credits:*</b> 6	<b>Total Hours:</b> 180	<b>Self-study Hours:</b> 120	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The examination is performed in form of an oral exam (30mins; applied when the course has less than 20 students) or a written exam (120mins; applied when the course has 20 or more students). The exam will cover tasks conducted before in the hands-on sessions/exercises (which in turn, cover the main content of the lecture in a practical fashion). The tasks/exercises allow to evaluate how well the students understood the respective concepts and how well they can implement corresponding algorithms for logic synthesis and physical design.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Programming skills

#### Content:

Modern computer chips consist of billions of transistors, making them some of the most complex systems ever created by humans. How does one design such intricate architectures? The answer is algorithms developed and fine-tuned over decades. In this course, students will learn about the techniques that automatically obtain computer chip designs from specifications. To this end, we will explore logic synthesis and optimization as well as partitioning, floorplanning, placement, and routing. Many of these algorithms are meta-heuristics that can be applied in completely different fields, too, like resource allocation, city planning, logistics, compilers, etc. Additionally, students will

gather hands-on experience with state-of-the-art tools in logic synthesis and physical design, with the opportunity to participate in an international contest.

The students will get to know data structures and algorithms, and will be able to implement them, e.g.,

- AIGs, MIGs, XAGs, kLUT networks,
- logic optimization and technology mapping,
- combinational equivalence checking,
- floor planning,
- global and detailed placement,
- global and detailed routing,
- legalization.

Additionally, the students will learn to operate open-source industrial-strength tools in the field, like ABC, Yosys, OpenROAD, or iEDA.

### **Intended Learning Outcomes:**

At the end of the module, students will have

- a detailed insights into how synthesis, optimization, and physical design algorithms work,
- an understanding of different data structures and core methods for software tools,
- the ability to properly apply synthesis, optimization, and physical design tasks,
- the capability to extend software tools with novel or existing algorithms, and
- be able to use tools considered in the lecture (e.g., ABC, Yosys, OpenROAD, or iEDA).

### **Teaching and Learning Methods:**

The module will be held in the form of presentations about the topics covered above followed by corresponding hands-on sessions/exercises. Using slides presentations and whiteboard sketches, the main concepts of the respectively considered topics are provided. In addition, the students will have the opportunity to deepen their knowledge through individual hands-on experiences with corresponding software tools.

### **Media:**

Lecture slides, software tools.

### **Reading List:**

- \* Lengauer, T. Combinatorial Algorithms for Integrated Circuit Layout. Springer, 1990.
- \* De Micheli, G. Synthesis and Optimization of Digital Circuits. McGraw-Hill Professional, 1994.
- \* Leighton, F. T. Complexity Issues in VLSI. MIT Press, 2003.
- \* Alpert, C. J., Mehta, D. P., Sapatnekar, S. S. Handbook of Algorithms for Physical Design Automation. Auerbach Publications, 2008.
- \* Kahng, A. B., Lienig, J., Markov, I. L., Hu, J. VLSI Physical Design: From Graph Partitioning to Timing Closure, 2nd ed. Springer, 2022.

### **Responsible for Module:**

Wille, Robert; Prof. Dr.-Ing.

**Courses (Type of course, Weekly hours per semester), Instructor:**

Logic Synthesis and Physical Design (Vorlesung mit integrierten Übungen, 4 SWS)

Walter M, Wille R

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### CIT433033: Design of Digital Circuits | Design of Digital Circuits [DDC]

Version of module description: Gültig ab winterterm 2025/26

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 90	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

In a written exam (60 min), students demonstrate by answering text questions and calculating tasks that (i) they can correctly reproduce the concepts of digital circuit technology and their physical relationships and that (ii) they can apply the knowledge they have learned to solve typical problems in the field of digital design. The assignments test the achievement of the learning objectives, in particular with regard to the topics of time and power behavior of circuits, memory technologies, fault tolerance, and current concepts for the implementation of basic components of digital circuits.

In addition, students can achieve a voluntary grade bonus of 0.3 on the final grade by successfully completing the homework assignments (3 to 5 tasks). With these tasks, students demonstrate in particular their knowledge of the design process of digital circuits and their ability to transfer theoretical concepts into practice.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Basic knowledge of working principals of transistors and Boolean algebra at Bachelor level is required.

#### Content:

This module explains key concepts that are used in current digital design for integrated circuits. Based on fundamental physical relationships, the properties of digital circuits with regard to power consumption and time behavior are investigated and design methods for these purposes are discussed. Based on known basic circuits, current concepts for the implementation of typical components of digital circuits are discussed and their implementation variants are derived. The relationship between the description of these concepts in a hardware description language and the

implementation in an integrated circuit is also discussed, whereby the various steps of the design process are also considered.

In addition to the theoretical part of the content in lectures, the practical relevance is illustrated with exercises and homeworks.

### **Intended Learning Outcomes:**

After successfully completing this module, students will have acquired the following qualifications:

- They understand causes of power dissipation in digital circuits and techniques to reduce power dissipation and will be able to apply these techniques in the design of digital circuits.
- They understand the differences between synchronous and asynchronous implementations of digital circuits, can determine the timing behavior of digital circuits, and can apply methods for synchronization between clock domains.
- They understand the structure of different memory technologies and can apply this knowledge to make a suitable choice when developing circuits.
- They know the principles of fault tolerance and can evaluate them.
- They know the basic elements of digital circuits such as state machines, FIFOs, adders and multipliers, understand current concepts for their implementation, and can evaluate which concepts are suitable in a given scenarios.
- They know the steps of the design process and understand the relationships between a description in a hardware description language and the resulting circuit.

### **Teaching and Learning Methods:**

Knowledge is conveyed by means of slides and blackboard notes. The students' learning process is supported in the exercises by interactive solutions to tasks. Practical homework during the semester helps to deepen and illustrate the knowledge acquired.

### **Media:**

Slides, blackboard work, sample code, and interactive online tools, e.g. questionnaires, are used in lectures and exercises. The offer is supplemented by a forum on Moodle, where lecturers answer questions about the content and practical tasks.

### **Reading List:**

- Niklaus Wirth; Digital Circuit Design for Computer Science Students - An Introductory Textbook; Springer; 1995 ISBN 978-3-540-58577-0
- H. Lipp, J. Becker, "Grundlagen der Digitaltechnik", Oldenbourg
- H. Klar, "Integrierte Digitale Schaltungen MOS/BICMOS", Springer
- U. Tietze, C. Schenk, "Halbleiter-Schaltungstechnik", Springer
- J. Rabaey, "Digital Integrated Circuits - A Design Perspective", Prentice Hall
- J. Wakerly, "Digital Design Principles and Practices", Prentice Hall

Further literature may be given in the Moodle course for the lecture.

**Responsible for Module:**

Pehl, Michael; PD Dr.-Ing. habil.

**Courses (Type of course, Weekly hours per semester), Instructor:**

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### EI50141: Testing Digital Circuits | Testing Digital Circuits [TDC]

Version of module description: Gültig ab winterterm 2019/20

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 105	<b>Contact Hours:</b> 45

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The examination will be in an oral, highly interactive and dynamic form (30 mins). The student will show his/her ability to understand, apply, develop and evaluate test solutions for digital integrated circuits and systems, at the concrete example of a small digital circuit with single stuck-at faults. In detail, he/she will compute test patterns and develop parts of a scan path and of a built-in self-test. While doing so, the student will present his/her understanding of the underlying algorithms and methods, as there are e.g. D-algorithm, test complexity analysis, IEEE 1149.1 boundary scan testing, memory testing, IDDQ testing.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Basics of digital circuit design.

The following modules should be passed before taking the course:

- Digital IC-Design
- Electronic Design Automation

#### Content:

Principles of testing digital circuits; fault models and test quality; functional and structural test generation; fault simulation; complexity theory; design for test (passive, active test methods); memory test; test standards; miscellaneous topics (Iddq test, analog test, test pattern compression, yield management);

In detail:

The manufacturing process of integrated circuits introduces a large variety of physical defects. In order to prevent the delivery of failing silicon devices to the customer, the correct function of

delivered integrated circuits has to be guaranteed by testing all devices after they have been fabricated.

Testing integrated circuits is one of the core competencies of a semiconductor company. It represents a significant factor in costs and quality. Therefore, testing is considered as an outstanding part of the entire design and manufacturing process of ICs.

Furthermore, testing is a domain-crossing topic: The test engineer within a semiconductor company requires a broad expertise covering circuit and system design, circuit simulation and design verification, and physical design.

One of the main challenges in testing is costs which have drastically increased over the past years. The access to circuit internal transistors and nodes has to be accomplished by a limited number of external pins. This is increasingly difficult due to the continuous shrinking of device structures.

This lecture conveys:

- \* The basic idea of testing.
- \* Relevant failure mechanisms of integrated circuits and the common fault models.
- \* The complexity problem of testing and its resulting limitations.
- \* Methods for test pattern generation (e.g. fault simulation and automatic test generation).
- \* Fundamental measures for designing integrated circuits in order to raise their testability (Design-for-Testability).
- \* Techniques for insertion of built-in self-test (BIST) in integrated circuits.
- \* Techniques for memory testing.

### **Intended Learning Outcomes:**

Intended Learning Outcomes

At the end of the module students know about the following topics and are able to employ this knowledge to define and evaluate test solutions for digital ICs and systems:

- Definition of testing and the difference to verification
- Fundamentals of testing: fault models, fault detection, redundant faults, fault coverage
- Methods for test generation: Boolean differences, D-algorithm, fault simulation
- Analysis of test complexity with the help of complexity theory
- Principles of passive test methods: Ad-hoc measures, scan path / Principles of active test methods: BIST
- Overview over memory fault models and memory test algorithms.
- Outline of test standards (IEEE boundary scan test) and additional topics like IDDQ testing, analog testing, fault analysis

### **Teaching and Learning Methods:**

Learning method:

In addition to the individual methods of the students consolidated knowledge is aspired by repeated lessons in exercises and tutorials.

**Teaching method:**

During the lectures students are instructed in a teacher-centered style. The exercises are held in a student-centered way.

Where applicable, each of the 10 chapters of the lectures is immediately followed by an associated exercise/tutorial block.

**Media:**

The following kinds of media are used:

- \* Presentations
- \* Handouts of the presentations and additional lecture notes
- \* Handouts of exercises

**Reading List:**

The following literature is recommended:

- \* Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits; M. Bushnell, V. Agrawal; Kluwer Academic Publishers, 2000.
- \* Digital Systems Testing and Testable Design; M. Abramovici, M. Breuer, A. Friedmann; Computer Science Press, 1990

**Responsible for Module:**

Schlichtmann, Ulf; Prof. Dr.-Ing.

**Courses (Type of course, Weekly hours per semester), Instructor:**

Testing Digital Circuits (Vorlesung mit integrierten Übungen, 3 SWS)

Otterstedt J, Lian M

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### EI70610: Electronic Design Automation | Electronic Design Automation [EDA]

Version of module description: Gültig ab winterterm 2024/25

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> summer semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 90	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

Written examination (75 minutes, open book policy, non-programmable calculator permitted) (100%) with questions that check the knowledge of synthesizing, optimizing and simulating digital circuits on logic level and the capability of modeling electronic design tasks mit mixed integer linear programming.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Fundamentals of digital logic design; fundamental engineering mathematics;

#### Content:

Logic Synthesis: Boolean functions, synthesis of 2-level combinational circuits, heuristic minimization of 2-level combinational circuits, synthesis of multi-level combinational circuits, ordered binary decision diagrams, synthesis of sequential circuits with finite state machines (FSM);

Logic Simulation: event-driven simulation, modeling and simulation using VHDL;

Mixed Integer Linear Programming (MILP) Modeling: properties of modeling method, mathematical modeling techniques (constraint linearization, OR-relation transformation, propositional logic modeling, absolute value modeling), modeling common EDA problems including grid routing, gridless routing, escape routing on printed circuit board (PCB), area routing on PCB, non-overlapping placement, area minimization, network flow, etc.

Additional Topics: modeling applications in emerging technologies.

**Intended Learning Outcomes:**

Upon successful completion of the module students are capable of employing algorithms for computer-aided design of (digital) integrated circuits, electronic systems, and other emerging platforms. Students can use and develop software tools for synthesis, optimization and simulation of digital circuits on logic level. They are capable of modeling tasks of electronic design automation as mixed integer linear programming problems.

**Teaching and Learning Methods:**

Learning method:

In addition to the individual learning of the students, consolidated knowledge is acquired by exemplary solutions to exercises and examples in the lectures.

Teaching method:

Students are instructed by blackboard writing, interactive discussions, sometimes slide presentations and enactment of solving exemplary tasks.

**Media:**

The following kinds of media are used:

- Blackboard presentations
- Comprehensive collection of formulas and algorithms
- Catalog of exercises with solutions
- Additional examples and demos are available online

**Reading List:**

The following literature is recommended:

- Algorithms for VLSI Design Automation; Sabih H. Gerez; John Wiley & Sons 1999
- Synthesis and Optimization of Digital Circuits; De Micheli, Giovanni; McGraw-Hill 1994
- VLSI Physical Design Automation; S. Sait, H. Youssef; McGraw-Hill 1995
- Applied Mathematical Programming; Bradley, Hax, and Magnanti; Addison-Wesley 1977

**Responsible for Module:**

Schlichtmann, Ulf; Prof. Dr.-Ing.

**Courses (Type of course, Weekly hours per semester), Instructor:**

Electronic Design Automation (Automatisierung des Entwurfs elektronischer Systeme) (Vorlesung mit integrierten Übungen, 5 SWS)

Tseng T, Li M, Fengler P, Schlichtmann U

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### EI70630: HW/SW Codesign | HW/SW Codesign

Version of module description: Gültig ab summerterm 2022

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter/summer semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 105	<b>Contact Hours:</b> 45

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The exam (written, 75 minutes) is adjusted to the different topics conveyed. Acquired knowledge will be tested in different ways: The students have to remember the properties of the conveyed concepts and algorithms used in the different steps of the design flow, they have to apply associated algorithms to given design problems and they have to analyze design problems and associated given solutions.

The final grade is made up exclusively by the final exam.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

No specific requirements.

#### Content:

The module covers the design flow from a system specification in form of function graphs down to FPGA netlists and executable object code for microprocessors with special focus on the partitioning of sub-functions into a software and a hardware part of a System-on-Chip (SoC). The major topics are: modeling and specification of mixed hardware/software solutions for embedded systems, graph partitioning and binding to execution units, scheduling of tasks, estimation of design quality.

#### Intended Learning Outcomes:

At the end of the module students are able to understand specification and modeling of mixed hardware-/software solutions, the optimized partitioning of sub-tasks into hardware or software partitions and their binding to specific processing entities as well as the scheduling of these tasks

as the major problems in the design of combined HW/SW systems. They will be able to apply the standard method of a top down design flow consisting of specification, exploration and refinement.

Further, the students will be able to use different algorithms like hierarchical clustering, group migration, simulated annealing or tabu search for partitioning and various algorithms for static and dynamic scheduling that help in solving them.

In addition, they will be able to evaluate the design quality reached by applying these approaches and tailor them to specific problems for creating own SoC architectures.

**Teaching and Learning Methods:**

The basic learning method is presentation during the lecture, supplemented with group discussions. During the tutorial the solution of example problems will be discussed. For a better understanding students will read scientific publications as self studies. Case studies will be discussed to get a practical understanding of the problems to be solved for HW/SW codesign of embedded systems / Systems-on-Chip.

**Media:**

Presentation slides and lecture notes.

The lecture is given in English.

**Reading List:**

D. Gajski, "Specification and Design of embedded Systems", Prentice Hall

**Responsible for Module:**

Herkersdorf, Andreas; Prof. Dr.

**Courses (Type of course, Weekly hours per semester), Instructor:**

HW/SW Codesign (Vorlesung mit integrierten Übungen, 3 SWS)

Kantic J [L], Herkersdorf A, Wild T, Stechele W, Kantic J

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### EI70730: Memory Technology for Data Storage | Memory Technology for Data Storage [EINEU008]

Version of module description: Gültig ab summerterm 2020

<b>Module Level:</b> Master	<b>Language:</b> German/English	<b>Duration:</b> one semester	<b>Frequency:</b> winter/summer semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 90	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

60 minutes examination with the following elements:

- Written examination, closed books, no notes
- It consists of questions that cover the knowledge of all the diverse memory technologies that have been explained, hand calculations and drawings that cover the ability to solve and explain problems arising from the used technologies and related background questions. Examples for typical exam questions are the questions in the exercises.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Basic Physical concepts, materials, electronic devices

The following modules should be passed before taking the course:

- Physik für Elektroingenieure
- Werkstoffe der Elektrotechnik
- Elektronische Bauelemente

#### Content:

Without memory technologies we would not be able to live our connected lifestyle. Memory is the core of our tablets, PCs, smart phones, servers, cloud services, deep learning hardware and the basis of almost all complex electronics. Understanding how different memory technologies work and where their limitations are is crucial for most applications.

Memory technology operates at the forefront of semiconductor technology and production.

Memory technology uses the most advanced lithography tricks and the latest transistor designs

in combination with novel electronic materials. Therefore, you will touch base with the latest challenges in nanoelectronics and learn how to live with them or how to mitigate them.

The lecture will discuss technology details, limitations and challenges along the memory hierarchy in data storage systems.

Outline:

semiconductor memories:

- SRAM
- DRAM
- Soft errors (SER)
- Flash
- FeRAM
- MRAM
- PCRAM (3D XPoint)
- OTP like e-Fuse, Antifuse, eMemory, Kilopass, Synopsys, NSCore

Emerging Memories:

- resistive memory technologies (Memristor etc.)
  - 3D memory technologies
  - mechanical and magnetic memories:
    - magnetic tape storage
- historical memory devices

### **Intended Learning Outcomes:**

After completion of this course, the student

- understands advanced patterning, litho and layout techniques
- understands advanced transistor concepts like FinFet, Gate-all-Around FET, FD-SOI and MCBFETs
- knows the economic and performance aspects of the memory hierarchy (evaluate)
- is able to evaluate pros and cons of different memory technologies
- knows which memory to choose for a given application (apply)
- knows what technology to choose for having memory w/o extra masks (apply)
- knows a metric how to benchmark different memory technologies (evaluate)
- knows the physical limitation for each memory technology (evaluate)
- knows the physical challenges for each technology (evaluate)
- understands the basic physics and technology for semiconductor memories
- understands the basic physics and technology for magnetic storage
- understands the basic physics and technology of insulators, high-k and metal gate materials
- understands the basic physics and technology for phase-change materials for data storage
- knows architecture-based limitations of certain memory technologies (evaluate)
- has an overview of current nano-electronic challenges

### **Teaching and Learning Methods:**

Lecture with discussion

readings assignments, case studies

### Individual and group exercises

In addition to the individual student's methods a consolidated knowledge is targeted by repeated lessons in exercises and tutorials.

### Teaching method:

During the lectures students are instructed in a teacher-centered style. The exercises are held in a student-centered way.

### Media:

e-learning Moodle

### Reading List:

The Art of Assembly Language, Randy Hall, eBook: <http://www.plantation-productions.com/Webster/www.artofasm.com/index.html>

Volume 2: The basic system components

Volume 2: Memory architecture 6.1 - 6.6

Memory Systems: Cache, DRAM, Disk. Bruce Jacob, Spencer W. Ng, and David T. Wang, with contributions by Samuel Rodriguez. ISBN 978-0-12-379751-3, Morgan Kaufmann Publishers, September 2007

Individual handouts and scripts on Moodle

### Responsible for Module:

Kreupl, Franz; Prof. Dr. rer. nat.

### Courses (Type of course, Weekly hours per semester), Instructor:

Memory Technology for Data Storage (Vorlesung mit integrierten Übungen, 4 SWS)

Kreupl F

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Analog/Mixed-Signal Design | Analog/Mixed-Signal Design

### Module Description

#### **CIT433030: Fundamentals of CMOS Technology for Analog Design and Standard Cell Libraries | Fundamentals of CMOS Technology for Analog Design and Standard Cell Libraries [Fundamentals-CMOS]**

*Fundamentals of CMOS Technology for Analog Design and Standard Cells*

Version of module description: Gültig ab winterterm 2025/26

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 6	<b>Total Hours:</b> 180	<b>Self-study Hours:</b> 120	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### **Description of Examination Method:**

The exam is in a written form and it lasts 75min. The exam includes questions about the principles of CMOS technology and the basic operations of transistors as well as concepts of analog circuits and standard cells. Different CMOS technologies will be covered. In addition, problems to test the understanding of how changes in operating conditions such as voltage and temperature impact the figure of merits of circuits like power, performance, and delay. These problems cover extensive topics related to how standard cells can be optimized and how reliability degradation like variation impact analog circuits.

#### **Repeat Examination:**

Next semester

#### **(Recommended) Prerequisites:**

Basic knowledge in circuits  
Basic knowledge in transistors

#### **Content:**

Fundamentals in CMOS technology.  
Fundamentals in standard cell design from both analog and digital perspective.  
Basic principles of MOSFET operations along with the key electrical parameters.  
Fundamentals in variability and temperature effects on transistor's operation and performance of analog circuits.  
Basics in layout for standard cells.

Basics of building standard cell libraries

**Intended Learning Outcomes:**

At the end of the module students know and understand the fundamental principles of CMOS technology. How different technologies (e.g., planer MOSFET, FDSOI, FinFET, nanosheet, etc.) impact the figure of merits of circuits. Students obtain a comprehensive knowledge and solid understanding of how standard cells work from analog and digital perspectives. Students know and understand the impact of variability, temperature, voltage on the reliability and performance of analog circuits and standard cells. In addition, student know in detail the key electrical parameters of transistors and how they impact circuits.

**Teaching and Learning Methods:**

The module includes lectures and tutorials. In the lectures, basic concepts and fundamental of CMOS technology and the relation to analog and standard cells. Visual aids such as PowerPoint slides, overhead projections and handwriting on black board are used. In each lecture, some concepts in CMOS technology and different challenges will be presented and discussed. Then discussions are held to explain and understand the transistor operation. In the tutorials, practical exercises of how transistors operate, SPICE simulations, standard cells design, basic concepts of standard cell libraries. Students also need to read scientific papers to discuss and challenge them for more comprehensive understanding. Students practice with small examples and thus get familiar with analog circuit simulations and standard cell design.

**Media:**

PowerPoint, black board, online materials, book chapter, scientific papers

**Reading List:**

- "Basics of CMOS Cell Design", ISBN: 9780070599338
- "CMOS Analog IC Design: Fundamentals" by Erik Bruun.
- "Nanometer CMOS ICs", ISBN: 978-3-031-64248-7
- selected scientific papers that will be shared with students

**Responsible for Module:**

Amrouch, Hussam; Prof. Dr.-Ing.

**Courses (Type of course, Weekly hours per semester), Instructor:**

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### CIT4430015: Analog and Mixed-Signal Circuit Design | Analog and Mixed-Signal Circuit Design [AMS]

Version of module description: Gültig ab winterterm 2023/24

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 75	<b>Contact Hours:</b> 75

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The assessment consists of a written final exam (60 minutes), in which students demonstrate their understanding of the fundamental concepts and structures of transistor-level integrated circuits and their ability to apply this knowledge—for example, by setting operating points, sizing small circuits, and tuning them to meet given specifications.

An optional mid-term exam (simulation or calculation task) is offered during the semester. If passed, it results in a bonus of 0.3 on the final grade, provided that the final exam is also passed.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

The course is intended for students holding a bachelor's degree in electrical engineering. A solid background in circuit and system theory, basic transistor-level circuit design, and solid-state and semiconductor device physics is highly recommended. A short refresher course covering these fundamentals will be offered during the first week of the semester.

#### Content:

1. Basics of CMOS process technology and device physics, essential for understanding and designing integrated circuits, including operating point setting and frequency response analysis.
2. Transistor-level integrated circuit design in CMOS technology, with focus on the structure and design challenges of key analog building blocks such as amplifiers, comparators, current and voltage references, clock generation, and voltage regulation circuits.
3. CMOS manufacturing non-idealities and their compensation in circuit design: optimization with respect to disturbances (parasitics, temperature and supply variations) and error sources (process variability, yield, noise).

**Intended Learning Outcomes:**

Upon successful completion of the module, students are able to understand the concepts and architectures of transistor-level analog and mixed-signal integrated circuits (ICs). They can describe the fundamental relationships between circuit specifications, device sizing, biasing, and circuit architecture.

Students gain a solid understanding of basic IC building blocks such as operational amplifiers, clock circuits, voltage references, comparators, regulators, and converters at the transistor level. They acquire the skills to design such circuits independently, with consideration of industrially relevant manufacturing aspects.

**Teaching and Learning Methods:**

The theoretical concepts are presented in weekly lectures, each beginning with a short Q&A session.

Weekly exercises for self-study are provided and discussed in a separate tutorial session. Circuit design software is also used to support a deeper understanding of the interaction between technology, transistor behavior, and its impact on circuits designed for practical applications.

**Media:**

Presentation slides, Moodle forum for discussions and announcements, exercise sheets with sample solutions, lecture notes and solutions from the tutorials.

**Reading List:**

B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill Education

**Responsible for Module:**

Brederlow, Ralf; Prof. Dr.-Ing.

**Courses (Type of course, Weekly hours per semester), Instructor:**

Analog and Mixed-Signal Circuit Design (Vorlesung mit integrierten Übungen, 5 SWS)

Brederlow R, Ahrens H, Schewa M, David K

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### CIT443020: Microstructured Devices in Micro and Power Electronics | Bauelemente der Mikro- und Leistungselektronik [DEV-MEPE]

Version of module description: Gültig ab winterterm 2025/26

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter/summer semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 105	<b>Contact Hours:</b> 45

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

This module will be assessed in a written final examination (60 min) after the teaching weeks. In this examination it is to verify that the candidates are able to understand the general principles of electronic devices, the related circuits and systems in the field of micro- and power electronics, to solve relevant problems in the fields covered in this module in a limited time and without any resources. The examination will cover all parts of the lectures and exercises of this module.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Basic knowledge in physical electronics, electrical engineering and the fundamentals of electronic devices as well as in semiconductor physics.

#### Content:

Application Fields of microstructured devices, Electronic and Power devices and requirements on those devices for practical application

Physical effects in solid-state microstructured electronic devices

Material properties of semiconductors

Phenomenological transport theory

Microelectronics

Power electronic devices

Selected types of microsensors and actuators and their application

Selectec aspects of reliability and ruggedness of electronic devices

### **Intended Learning Outcomes:**

After successful completion of the module, students are able to

- understand and apply the physical principles of electronic devices, circuits and systems in the field of micro- and power electronics
- are able to explain the operation of those devices and their application in the field
- have acquired profound knowledge and understanding of some of the problem-solving methods of devices, circuits and systems in the field of micro- and power electronics.

### **Teaching and Learning Methods:**

Teaching methods during the lectures and exercises:

Teacher-centered style with presentations and explanations on the blackboard.

In solving relevant exercises a deeper knowledge of the subject matters of the lessons is sought.

Language of instruction: German in Winter Semester/ English in Summer Semester

### **Media:**

The following media types are used in the lectures and exercises:

- Presentations (these are also offered as handouts for the students)
- Explanations and exemplifications on the black board
- Exercises are provided with the objective that the students first should solve the problems independent by themselves, the solutions to the problems will be demonstrated in subsequent exercise sessions.

### **Reading List:**

Simon M. Sze - Physics of Semiconductor Devices, 2nd Edition

J. Wiley (New York); 1998

- J. Lutz, H. Schlangenotto, U. Scheuermann, R. de Donker -

Semiconductor Power Devices; Springer Verlag; 2018

- S. Lindner - Power Semiconductors; EPFL Press; 2006

### **Responsible for Module:**

Schrag, Gabriele; Prof. Dr.

### **Courses (Type of course, Weekly hours per semester), Instructor:**

Bauelemente der Mikro- und Leistungselektronik (Vorlesung mit integrierten Übungen, 3 SWS)

Schrag G, Leikam B

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### CIT443021: Analog Bipolar Electronics: Devices, Simulation and Circuits | Analoge Bipolartechnik: Bauelemente, Simulation und Schaltungen [Bipolar]

*Analog Bipolar Electronics*

Version of module description: Gültig ab summerterm 2025

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> summer semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 105	<b>Contact Hours:</b> 45

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The module is examined in the form of an oral exam (20 min). The students must be able to demonstrate their insight into the functional dependencies and the fundamental properties of the analog bipolar technology and into their applications for high frequency circuits. A bonus of 0.3 will be applied to those who have solved more than 50% of the exercise tasks. The exercises are voluntary.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Basic lectures in circuit and system theory, electronic circuit design, solid-state and semiconductor device physics for bipolar transistors.

#### Content:

The lecture covers basic understanding of bipolar transistors and transistor circuits. Starting with the structure and characterization of Si bipolar transistors (BJT) and SiGe heterobipolartransistors (HBT) (corner frequencies, noise behavior), device parameters for circuit simulation are discussed, the fundamental circuits in bipolar technology (differential amplifiers, voltage references, translinear circuits) and their circuit performance is discussed, circuit topologies for high-speed analog and digital bipolar circuits (amplifiers, oscillators, multipliers, frequency dividers) will be introduced.

#### Intended Learning Outcomes:

The students are able to describe, analyse and develop simple designs of bipolar technology, devices and circuits for the highest frequencies in accordance to the state of the art.

### **Teaching and Learning Methods:**

The course will discuss the concepts and theory in weekly lectures with Q&A session at the beginning of each lecture.

Excercises for self study are given regularly and will be discussed in a separate session just after the lecture. Here we will also use a circuit simulation tool to support better understanding of the interaction between theoretical modeling and the behavior of circuits build for practical applications.

### **Media:**

The following media forms are used:

- Slide presentations
- Handout of the slides
- Examples written on the board

### **Reading List:**

1. Gray, Paul R., Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer. Analysis and design of analog integrated circuits. John Wiley & Sons, 2024.
2. Reisch, Michael. High-Frequency Bipolar Transistors. Vol. 11. Springer Science & Business Media, 2012.
3. Hareme, D. L., J. H. Comfort, J. D. Cressler, EFI Crabbe, JY-C. Sun, B. S. Meyerson, and T. Tice. "Si/SiGe epitaxial-base transistors. I. Materials, physics, and circuits." IEEE Transactions on Electron Devices 42, no. 3 (1995): 455-468.
4. Reisch, Michael. Elektronische Bauelemente: Funktion, Grundsaltungen, Modellierung mit SPICE. Springer-Verlag, 2013.

### **Responsible for Module:**

Dr. Pengcheng Xu

### **Courses (Type of course, Weekly hours per semester), Instructor:**

Analoge Bipolartechnik: Bauelemente, Simulation und Schaltungen (Vorlesung, 3 SWS)

Aufinger K, Wohlmuth H, Snoeij M, Schäffer V, Schewa M, Brederlow R

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### EI70710: Advanced Electronic Devices | Advanced Electronic Devices

Version of module description: Gültig ab summerterm 2025

<b>Module Level:</b> Master	<b>Language:</b> German/English	<b>Duration:</b> one semester	<b>Frequency:</b> summer semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 105	<b>Contact Hours:</b> 45

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

written (60 min.);

The written exam is composed of calculation exercises and short questions about the entire lecture contents, it serves as an examination of the basic understanding of important, non-ideal effects in diodes and field effect transistors as well as of an advance knowledge of architecture, function and application of specific, modern electronic devices. Up to 20% of the exam may comprise ticking boxes of multiple choice answers.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Basic knowledge about electronic devices

#### Content:

DIODES: ideal p-n-junction, metal-semiconductor contact, heterojunction, non-ideal effects (recombination and generation in the space charge region, high injection, finite-length leads), negative differential resistance devices (tunnel diode, resonant tunnel diode, Gunn diode), TRANSISTORS: classical MOSFET, scaling and short channel effects, High-Electron-Mobility-Transistor (HEMT), advanced MOSFETs (SOI, multiple gate, strained Si, metal gate, high-k dielectrics), low-dimensional transistors (nanowires, CNT, SET), organic field effect transistors (OFET, SAMFET)

#### Intended Learning Outcomes:

Basic understanding of important, non-ideal effects in diodes and field effect transistors; advance knowledge of architecture, function and application of specific, modern electronic devices; Ability to evaluate novel and future device developments in particular regarding their application potential.

**Teaching and Learning Methods:**

In addition to classical lecture presentation and individual study methods of the students exercises and additional tutorials will be provided, targeting at a deeper level of understanding. The students will get in early contact with current research topics.

**Media:**

The following media will be used: lectures, handouts, blackboard, tablet PC, lab visits

**Reading List:**

S. M. Sze, K.K. Ng, Physics of Semiconductor Devices , 3rd Ed. (2007), Wiley  
D.L. Pulfrey, ""Understanding Modern Transistors and Diodes"", (2010), Cambridge

**Responsible for Module:**

Becherer, Markus; Prof. Dr.-Ing. habil.

**Courses (Type of course, Weekly hours per semester), Instructor:**

Moderne Elektronische Bauelemente (Vorlesung mit integrierten Übungen, 3 SWS)

Ahrens V ( Becherer M )

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Specialized Elective Modules | fachliche Vertiefung

### Module Description

#### CIT4330012: Software for Quantum Computing | Software for Quantum Computing [Quantum SW]

Version of module description: Gültig ab summerterm 2024

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 105	<b>Contact Hours:</b> 45

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The examination is performed in form of either an oral (30 mins) or a written exam (90 mins). The exam will cover tasks conducted before in the hands-on sessions/exercises (which in turn, cover the main content of the lecture in a practical fashion). The tasks/exercises allow to evaluate how well the students understood the respective concepts and how well they can realize corresponding (software) methods for quantum computing.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Basic knowledge in programming (e.g., in Python, C++, etc.)

Basic knowledge in the use of design tools such as compilers, debuggers, etc.

#### Content:

Quantum computers have the potential to solve certain tasks that would take millennia to complete even with the fastest (conventional) supercomputer. Numerous quantum computing applications with a near-term perspective (e.g., for finance, chemistry, machine learning, optimization) and with a long-term perspective (i.e., cryptography, unstructured search) are currently investigated. However, while impressive accomplishments can be observed in the physical realization of quantum computers, the development of automated methods and software tools that provide assistance in the design and realization of applications for those devices is at risk of not being able to keep up with this development anymore. This may lead to a situation where we might have powerful quantum computers but hardly any proper means to actually use them.

This module provides an in-depth introduction into the internals of quantum computing software. This includes

- \* an elaboration on the differences between classical computing and quantum computing,
- \* an introduction to the design flow for quantum computing applications,
- \* a detailed coverage of data-structures and methods dedicated to quantum computing,
- \* a detailed coverage of software tools and methods for important design tasks such as quantum circuit simulation, quantum circuit compilation, quantum circuit verification, etc., as well as
- \* corresponding hands-on experiences of those tools considering actual quantum algorithms as well as quantum computing platforms.

### **Intended Learning Outcomes:**

At the end of the module, students will have detailed expertise of software for quantum computing with which corresponding applications can be realized. More precisely, they will

- \* understand the paradigm of quantum computing and will be able to evaluate how it differs from classical computing,
- \* be able to analyze whether an application is suited for quantum computing,
- \* be able to utilize and, if necessary, extend different data-structures as well as core methods that provide the basis for quantum computing software tools,
- \* be able to utilize and, if necessary extend software solutions for quantum computing (e.g., for quantum circuit simulation, quantum circuit compilation, and quantum circuit verification), as well as
- \* be able to realize, simulate, compile, verify, and execute quantum circuits using this software.

### **Teaching and Learning Methods:**

The module will be held in the form of presentations about the topics covered above followed by corresponding hands-on sessions/exercises. Using slides presentations and whiteboard sketches, the main concepts of the respectively considered topics are provided. In addition, the students will have the opportunity to deepen their knowledge through individual hands-on experiences with corresponding software tools.

### **Media:**

Lecture slides, software tools.

### **Reading List:**

M. A. Nielsen, I. L. Chuang: Quantum Computation and Quantum Information. Cambridge University Press (2010)

A. Zulehner and R. Wille. Introducing Design Automation for Quantum Computing. Springer, 2020.

### **Responsible for Module:**

Wille, Robert; Prof. Dr.-Ing.

### **Courses (Type of course, Weekly hours per semester), Instructor:**

Software for Quantum Computing (Vorlesung mit integrierten Übungen, 3 SWS)

Wille R [L], Wille R

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### CIT4330016: Innovative Computing for AI | Innovative Computing for AI [IC4AI]

Version of module description: Gültig ab winterterm 2024/25

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 6	<b>Total Hours:</b> 180	<b>Self-study Hours:</b> 120	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The exam is in written format and lasts 75 minutes. The exam includes questions about the principles of technology scaling and the fundamental limitations along with the new concepts that become necessary in computer architecture to overcome those limitations and continue technology scaling. In addition, problems to test the understanding of how such fundamental limitations impact the performance, reliability, power and temperature of processors as well as what are the advantages and shortcomings of the different proposed solutions to improve technology scaling. These problems cover extensive reliability-related and energy-related topics of digital circuits and the underlying mechanisms that induce degradations in digital circuits.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Basic knowledge of computer architecture

Basic knowledge of digital circuits

#### Content:

Fundamental limits in technology scaling and why innovative computing methods are highly required.

Emerging beyond-CMOS technologies and their impact on the performance and energy of modern computing systems.

Emerging non-volatile memories and challenges in such new nano-scaled devices with respect to reliability, endurance, energy, etc.

Novel architectures beyond traditional von-Neumann principles.

In-Memory Computing and Neuromorphic Computing.

Novel algorithms for brain-inspired computing like Hyperdimensional Computing.

Combining novel algorithms with novel architecture for ultra-efficient computing systems.  
Reliability challenges in the existing technologies and emerging technologies and architectures.  
Novel cooling solutions for advanced thermal managements.

**Intended Learning Outcomes:**

At the end of the module students know and understand the fundamental limitations in technology scaling and which novel concepts are needed to overcome those limitations. Students obtain a comprehensive knowledge and solid understanding of the novel methods for computing that go beyond traditional von-Neumann computer architecture principles. Students know and understand the need for novel and emerging technologies for both logic and memories. Student will understand the novel methods for performing advanced reliability management when emerging nanotechnologies are in use. In addition, student know in detail the concepts of innovative computing methods such novel in-memory computing, near-memory computing, neuromorphic computing, brain-inspired hyperdimensional computing.

**Teaching and Learning Methods:**

The module includes lectures and tutorials. In the lectures, basic concepts of novel computing paradigms, that go beyond traditional computer architectures, are discussed. Visual aids such as PowerPoint slides, overhead projections and handwriting on black board are used. In each lecture, some problems in technology scaling are explained first. Then discussions are held to predict possible solutions. Thereafter, state-of-the-art solutions from both academia and industry are shown. In the tutorials, the techniques introduced in lectures are demonstrated and potential challenges are discussed. The advantages and shortcoming of presented state-of-the-art solutions are evaluated together with the students. Students need to read scientific papers to discuss and challenge them. Students practice with small examples and thus get familiar with the techniques presented in the state of the art and how they work and can be implemented.

**Media:**

PowerPoint, black board, online materials, scientific papers.

**Reading List:**

Springer Book: "Beyond-CMOS Technologies for Next Generation Computer Design", ISBN 978-3-319-90384-2 e-ISBN 978-3-319-90385-9

Springer Book: "Emerging Technology and Architecture for Big-data Analytics", ISBN 978-3-319-54840-1

- Hennessy, Patterson: Computer Architecture - A quantitative Approach.
- selected scientific papers that will be share with students

**Responsible for Module:**

Amrouch, Hussam; Prof. Dr.-Ing.

**Courses (Type of course, Weekly hours per semester), Instructor:**

Innovative Computing for AI (Vorlesung mit integrierten Übungen, 4 SWS)  
Amrouch H, Thomann S

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### **CIT433023: Circuit Reliability for AI in Advanced Technologies | Circuit Reliability for AI in Advanced Technologies [CR4AI]**

*Circuit Reliability for AI in Advanced Technologies*

Version of module description: Gültig ab summerterm 2025

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> summer semester
<b>Credits:*</b> 6	<b>Total Hours:</b> 180	<b>Self-study Hours:</b> 120	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### **Description of Examination Method:**

The exam is in written format and lasts 75 minutes. In the exam, students will demonstrate that they are able to solve problems related to circuit's reliability and degradation effects. Students will analyze how different workloads such as AI can impact circuit's reliability and how technology scaling impact the circuit's reliability. Students will analyze the existing tradeoffs among performance, reliability, power and temperature of modern processors. Students will demonstrate they solve problems about reliability-related and energy-related topics of circuits and processors.

#### **Repeat Examination:**

Next semester

#### **(Recommended) Prerequisites:**

Basic knowledge of computer architecture

Basic knowledge of digital circuits

#### **Content:**

- Technology Scaling and the Ever-Increasing Challenges in Transistor's and Circuit's Reliability.
- Key Reliability Degradation Mechanisms: Impact of Aging Effects, Temperature Effects, Self-heating Effects, and Soft Error Effects on the Reliability of Circuits.
- Modeling and Investigating Reliability Degradations from Transistors to Complex Circuits.
- Reliability-Aware Circuit Design.
- Techniques to Improve the Reliability of Processors and Mitigate Degradation Effects.
- System-Level Management Techniques to Optimize Reliability in Multi-Core Processors.
- Impact of Emerging Technologies on the Reliability of Future Chips.

### **Intended Learning Outcomes:**

At the end of the module students know and understand the fundamental concepts of design for reliability for circuits in advanced technology nodes. Students understand how heavy workloads induced by AI applications negatively impact the circuits' reliability. Students obtain a comprehensive knowledge and solid understanding of the underlying key mechanisms which impact reliability circuits and transistors. Students obtain solid knowledge on how technology scaling and advanced technologies impact the circuit reliability. Students learn in detail about the various mechanisms, such as aging effects, temperature effects, soft errors, and self-heating effects which degrade the reliability of transistors in modern chips in sub-10nm technologies. Students master advanced techniques and methods for protecting circuits and on-chip systems against reliability degradations. The module covers how circuit's reliability can be investigated, modeled, improved, and managed at different abstraction levels starting from transistors to logic gates to complex circuits like processors all the way to the system level. Students learn how novel emerging technologies can help in improving the reliability of circuits in the future.

### **Teaching and Learning Methods:**

The module includes lectures and tutorials. In the lectures, basic and fundamental concepts of reliability degradations for circuits and transistors are discussed. Visual aids such as PowerPoint slides, projector, and handwriting on black board are used. In each lecture, some problems in circuit's reliability are explained first. Then, discussions are held to predict possible solutions. Thereafter, state-of-the-art solutions from both academia and industry are shown and discussed with students. In the tutorials, the techniques introduced in lectures are demonstrated and potential challenges are discussed. The advantages and shortcoming of presented state-of-the-art solutions are evaluated together with the students. Students need to read scientific papers to discuss and challenge them. Students practice with small examples and thus get familiar with the techniques presented in the state of the art and how they work and can be implemented.

### **Media:**

PowerPoint, black board, online materials, scientific papers.

### **Reading List:**

Research Papers and Journals.

Springer Book: "Circuit Design for Reliability", ISBN 978-1-4614-4078-9.

Springer Book: "Fundamentals of Bias Temperature Instability in MOS Transistors", ISBN 978-81-322-2508-9.

Springer Book: "Beyond-CMOS Technologies for Next Generation Computer Design", ISBN 978-3-319-90384-2 e-ISBN 978-3-319-90385-9

Springer Book: "Dependable Embedded Systems", ISBN 978-3-030-52017-5.

### **Responsible for Module:**

Amrouch, Hussam; Prof. Dr.-Ing.

### **Courses (Type of course, Weekly hours per semester), Instructor:**

Circuit Reliability for AI in Advanced Technologies (Vorlesung mit integrierten Übungen, 4 SWS)

Amrouch H, Thomann S, van Santen V

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### CIT433031: Machine Learning for Electronic Design Automation and Manufacturing | Machine Learning for Electronic Design Automation and Manufacturing [ML for DA]

Version of module description: Gültig ab winterterm 2024/25

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter/summer semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 105	<b>Contact Hours:</b> 45

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The examination is performed in form of an oral exam (30mins; applied when the course has less than 20 students) or a written exam (60mins; applied when the course has 20 or more students). The exam will cover tasks conducted before in the hands-on sessions/exercises (which in turn, cover the main content of the lecture in a practical fashion). The tasks/exercises allow to evaluate how well the students understood the respective concepts and how well they can implement corresponding machine learning algorithms for design automation and manufacturing.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Basic machine learning knowledge, basic programming knowledge, basic circuit design knowledge

#### Content:

The complexity of modern chips significantly impacts the cost and capabilities of design and manufacturing for traditional Design Automation Toolkits. This issue is exacerbated by the increased relevance of software and applications running on modern SoCs and their co-design. Current Design Automation methodologies often struggle to fully capture and optimize complicated designs or reduce them to the initial specification. However, advancements in data-driven algorithms, particularly in Machine Learning, can address these shortcomings. This course teaches how to apply Machine Learning to enhance and improve the chip design process.

This module provides an in-depth exploration of machine learning for design automation, including:

- \* Theory and application of machine learning algorithms
- \* In-depth exploration of recent machine learning methods suitable for design automation tasks

- \* Overview of topics, areas, and current industrial pain points in the semiconductor chain where a great availability of data exists
- \* Detailed coverage of data structures and state-of-the-art tools for tackling design automation
- \* Hands-on experiences of machine learning algorithms applied to design automation tasks

**Intended Learning Outcomes:**

By the end of the module, students will

- \* gain detailed insights into how machine learning can aid in the development, design, testing, and manufacturing of chips,
- \* understand which problems in chip design/manufacturing can be approached by data-driven methodologies and how to do so, and
- \* have learnt the essential requirements and best practices for introducing machine learning in a chip design/manufacturing industrial setting.

The course will also cover different data structures and core methods that may form the basis for AI-based software methodologies. Through hands-on experience, students will implement and adapt machine learning algorithms for design automation and manufacturing tasks.

**Teaching and Learning Methods:**

The module consists of presentations on the topics followed by hands-on sessions/exercises. Main concepts are delivered through slide presentations and whiteboard sketches, and students will have the opportunity to deepen their knowledge through individual hands-on experiences with corresponding algorithms and tasks.

**Media:**

Lecture slides, software tools.

**Reading List:**

Ren, Haoxing, and Jiang Hu, eds. Machine Learning Applications in Electronic Design Automation. Springer Nature, 2023.

Abu-Mostafa, Yaser S., Learning From Data: A short course, 2012.

LeCun, Yann, Yoshua Bengio, and Geoffrey Hinton. "Deep learning." nature 521.7553, 2015.

Karniadakis, George Em, et al. "Physics-informed machine learning." Nature Reviews Physics 3.6, 2021.

**Responsible for Module:**

Wille, Robert; Prof. Dr.-Ing.

**Courses (Type of course, Weekly hours per semester), Instructor:**

Machine Learning for Electronic Design Automation and Manufacturing (Vorlesung mit integrierten Übungen, 3 SWS)

Servadei L [L], Servadei L, Wille R

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### CIT433040: Embedded Systems and Security | Embedded Systems and Security [ESS]

Version of module description: Gültig ab summerterm 2025

<b>Module Level:</b> Master	<b>Language:</b> German/English	<b>Duration:</b> one semester	<b>Frequency:</b> winter/summer semester
<b>Credits:*</b> 6	<b>Total Hours:</b> 180	<b>Self-study Hours:</b> 90	<b>Contact Hours:</b> 90

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The examination consists of a written exam (90 minutes, 80% of the overall grade) and an exercise with programming tasks (20% of the overall grade). The two examination components test different learning outcomes:

The acquisition of the theoretical knowledge which is required to explain

- memory organization,
  - memory mapped I/O,
  - the purpose of discussed peripherals,
  - interrupts,
  - methods for separation,
  - MMUs/MPUs,
  - side channels,
  - the concept of trusted computing, to name
  - the discussed peripherals,
  - examples for typical vulnerabilities,
  - security objectives,
- and to
- classify types of on-chip memory,
  - recall the boot process of a uC,
  - compare methods for embedded debugging,
  - choose appropriate countermeasures,
  - discuss common attacks

is examined by open and closed questions in a written exam (90 min). The questions must be answered without aids by noting down key points or brief running text. The questions partly refer to given exemplary code. Calculations can be necessary for answering the questions. The grade for this part of the exam contributes to the grade of the module with 80%.

The practical capabilities to use

- tool chains for embedded development,
- memory mapped I/O,
- interrupts
- methods for embedded debugging
- cryptography

and to apply some common attacks is examined in form of 3 to 5 programming tasks. The grade for this part of the exam contributes to the grade of the module with 20%.

**Repeat Examination:**

Next semester

**(Recommended) Prerequisites:**

C programming  
Basic knowledge in computer architectures

**Content:**

- Introduction to micro controllers, differences to desktop computers
- Memory in embedded systems and its usage by C compilers
- Typical peripherals and their usage
- Interrupts and exceptions
- Embedded debugging
  
- Short introduction to security objective and cryptographic operations
- Typical vulnerabilities in embedded systems
- Common attacks and countermeasures
- A note on side-channels
- Concepts of separation and trusted computing

**Intended Learning Outcomes:**

The students are able to design a secure embedded system. In particular, to implement given tasks on an embedded system and to assess and choose appropriate measures to secure an embedded system. The former includes being able to

- Use tool chains for embedded development
- Discuss memory organization
- Classify types of on-chip memory
- Recall the boot process of a uC
- Describe and use memory mapped I/O
- List common peripherals and explain their purpose
- Explain and use interrupts
- Compare and use methods for embedded debugging

while the latter encompasses the ability to

- List security objectives
- Exemplify typical vulnerabilities
- Apply some common attacks
- Choose appropriate countermeasures
- Use cryptography
- Illustrate methods for separation
- Explain and use MMUs/MPUs
- Explain side channels
- Demonstrate the concept of trusted computing

**Teaching and Learning Methods:**

Knowledge will be taught using slides and notes on the blackboard. Learning by students is supported within the exercises through interactive problem discussion, group work and live programming of the tutor for exemplary security scenarios. Programming exercises regarding the implementation of security measures during the semester give students the opportunity to train and show their skills on real hardware, e.g. an ARM-platform.

Language of instruction: English in Winter Semester and German in Summer Semester.

**Media:**

Lecture as well as exercise sessions employ slides, working on the blackboard, and interactive online tools, e.g., questionnaires and etherpads. An additional Moodle forum, where teaching staff answers questions regarding content and programming exercises, complements the offer.

**Reading List:**

The definitive guide to ARM Cortex-M3 and Cortex-M4 processors  
Joseph Yiu

Understanding Cryptography  
Christoph Paar, Jan Pelzl  
Accompanied lecture slides: <http://www.crypto-textbook.com>

Handbook of Applied Cryptography  
Alfred J. Menezes, Paul C. van Oorschot, Scott A. Vanstone  
Download from: <http://www.cacr.math.uwaterloo.ca/hac/>

Security Engineering  
Ross Anderson  
Download from: <https://www.cl.cam.ac.uk/~rja14/book.html>

**Responsible for Module:**

Sigl, Georg; Prof. Dr.-Ing.

**Courses (Type of course, Weekly hours per semester), Instructor:**

Embedded Systems and Security (Übung, 2 SWS)

Nöpel J [L], Brosch M

Embedded Systems and Security (Praktikum, 1 SWS)

Nöpel J [L], Brosch M

Embedded Systems and Security (Vorlesung, 2 SWS)

Sigl G ( Nöpel J )

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### **CIT4430001: System Design for High-Frequency and High-Data Rate Applications | System Design for High-Frequency and High-Data Rate Applications [SDHA]**

*System Design for High-Frequency and High-Datarate Applications*

Version of module description: Gültig ab summerterm 2025

<b>Module Level:</b> Master	<b>Language:</b> German/English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 90	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### **Description of Examination Method:**

A written exam (90min) will be given at the end of the lecture period to test the required learning objectives.

In the written exam, students demonstrate that they have understood the basics of calculating circuits for transmission at high data rates and can independently design a system.

#### **Repeat Examination:**

Next semester

#### **(Recommended) Prerequisites:**

1. electronic circuits
2. communications engineering
3. introduction to high frequency technology

#### **Content:**

Today's world as an electronics engineer requires advanced knowledge on system design. With the requirement of high data-rates in many applications, circuits complexity heavily impacts the performance of a system. Special care must be taken when designing high-frequency or high-datarate applications. In this lecture course students will learn what to consider when designing such systems and how to design, simulate and evaluate a high-speed circuit.

The course is structured as follows:

1. Fundamentals of high frequency applications
  - a) Signal parameters
    - Risetime, Bandwidth, Overshoot, Jitter
  - b) Properties of signal sources and sinks

- Source-/Load-Impedance, Non-Linearity

c) Signals in circuits

- Signal loss, Frequency sensitivity, Impact on the signal form, Coupling and interference

2. System Layout

a) Material and Manufacturing

- Substrate selection, Physical and electrical properties, Parameter deviation

b) Conductor design and dimensioning

- Impedance matching, Conductor shape and geometry, Influence of loss on signal integrity, Track distance and Coupling

c) Via Layout

- Parasitic influence and quantitative estimation, Compensation

d) Layer stack for high data-rate

- Signal, Ground and supply layers, Limitations from manufacturing

3. System Design

a) Component selection

b) Power Supply Design

- Design rules, Stabilization and interference elimination

c) Signal Integrity

- Coexistence of analog and digital circuits

4. Simulation and Measurements

a) Simulation Tools

- Advanced Design System, CST

- Approximation, De-embedding, Layout validation

b) Measurements

- Time- and frequency-domain measurement methods

- Conductor parameter measurement

- Eye diagram

5. Application Specific Design

a) High-Speed Memory Interfaces

- Double Data Rate (DDR) RAM (Gen. 3/4/5)

- eMMC HS400

b) Peripheral Interconnect

- Peripheral Component Interconnect (PCI) Express (Gen. 1-4)

- JESD204A/B/C

### **Intended Learning Outcomes:**

After successful completion of the module, students gained basic knowledge on how to design, simulate, and evaluate advanced circuits for sensing and computing applications.

First, they are able to understand the fundamentals of high-frequency and high-datarate applications. Second, they know how the design and layout of schematics and printed-circuit boards is done and which aspects can be verified by simulation.

**Teaching and Learning Methods:**

The lecture introduces methods and tools for system design for high frequency and high data rate applications. In the tutorial students will learn how to calculate design specific parameters and individually experiment with the design tools provided.

**Media:**

- a) Lecture slides, scriptum, and laboratory manual.
- b) CAD with Altium Designer, CST/HFSS and ADS simulation tools.

**Reading List:**

RF Circuit Design, Second Edition(2nd Edition) by Christopher Bowick, John Blyler, Cheryl J. Ajluni  
High Speed Digital Design: A Handbook of Black Magic (Prentice Hall Modern Semiconductor Design) by H. Johnson, M. Graham

**Responsible for Module:**

Hagelauer, Amelie; Prof. Dr.-Ing.

**Courses (Type of course, Weekly hours per semester), Instructor:**

System Design for High-Frequency and High-Data Rate Applications (Vorlesung mit integrierten Übungen, 4 SWS)

Dorn C [L], Dorn C

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### CIT443018: Phase Locked Loop/Clocked Circuits | Phase Locked Loop/Clocked Circuits [PLL]

#### *Phase Locked Loop*

Version of module description: Gültig ab winterterm 2024/25

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 90	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### **Description of Examination Method:**

If the number of exam participators is below 40, we will have a final oral exam (20 min/student). Otherwise, we will have a final 60 min written exam. The students should demonstrate their insight into the basic concepts and system structures of phase locked loop and clocked circuits, as well as their ability to apply them to practical circuit design.

#### **Repeat Examination:**

Next semester

#### **(Recommended) Prerequisites:**

Solid-State and Semiconductor Device Physics, Analog and Mixed-Signal Electronics.

#### **Content:**

- a) Principle of Clocked Circuits
- b) Frequency Domain versus Time Domain
- c) Classes of Oscillators
- d) Clock Generation
- e) Clock Multiplication
- f) Phase Locked Loop
  - i. Modelling of Transfer Functions
  - ii. Noise Analysis
  - iii. System Considerations
  - iv. Digital & Analog
  - v. Integer & Fractional
- g) Phase Control
  - i. Digital Locked Loop

ii. Interpolators

**Intended Learning Outcomes:**

Upon successful completion of the module, students are able to understand the concepts and structures of PLL and Clocked Circuits. The students have an insight in the connection between theoretical modeling and the behavior of circuits. Students are able to describe basic interaction between circuit specifications and the sizing and structure of the circuit.

**Teaching and Learning Methods:**

The course will discuss the concepts and theory in weekly lectures with Q&A session at the beginning of each lecture. Exercises for self study are given weekly and will be discussed in a separate session. Here we will also use matlab to support better understanding of the interaction between theoretical modeling and the behavior of circuits build for practical applications.

**Media:**

MS PowerPoint Slides, Moodle, LTspice, Matlab

**Reading List:**

Design of CMOS Phase-Locked Loops: From Circuit Level to Architecture Level. Behzad Razavi

**Responsible for Module:**

Dr. Pengcheng Xu

**Courses (Type of course, Weekly hours per semester), Instructor:**

Phase Locked Loop/ Clocked Circuits (Vorlesung mit integrierten Übungen, 4 SWS)

Brederlow R, Dietl M, Xu P, Verma V

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### CIT443031: Power Management Integrated Circuits | Integrierte Schaltungen für das Leistungsmanagement [PMIC]

Version of module description: Gültig ab winterterm 2025/26

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 90	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

Written exam, duration: 60 minutes (100% of the final grade).

Students will be expected to demonstrate:

A solid understanding of the fundamental concepts, architectures and design trade-offs in power-management integrated circuits (PMICs), including voltage regulators, switches, power sequencing and protection circuits.

The ability to apply these concepts to the analysis and design of practical PMIC blocks (e.g., LDOs, switching converters, charge pumps) and system-level power management strategies.

The exam will consist of a mix of short-answer questions and design problems that test both theoretical insight and practical circuit design skills in the context of power-management ICs.

Short questions (definitions, conceptual explanations, etc.)

Schematic analysis (critical evaluation of given PMIC topologies, etc.)

Design tasks (sizing of components, stability considerations, efficiency calculations, etc.)

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Electronic circuits.

Analog and mixed-signal electronics.

#### Content:

Introduction & Use Cases

- The role of PMICs in electrical systems: placed between the energy source and the electronics
- Key requirements: size, efficiency, reliability, noise performance, cost
- Fundamental topologies:
  - Linear regulator (resistive approach)

- Inductor-based DC/DC converter (switch + inductor)
- Switched-capacitor converter (switch + capacitor)
- Hybrid converters (switch + capacitor + inductor)
- Power-management system architectures: multiple rails (e.g., Li-ion battery → DC/DC → analog LDO + digital LDO)

#### Power Devices & Components

- Power-stage configurations: low-side switch, high-side switch, half-bridge, full-bridge
- Non-ideal effects:  $R_{DSon}$ , dropout, parasitic capacitances, body diode
- Loss mechanisms: conduction losses, switching losses
- Passive components: MOS, MOM, MIM capacitors; planar inductors
- Power transistors: DEMOS, DMOS; SOI technologies; latch-up; safe-operating area (SOA); dead-time generation

#### Linear Regulators – Basics

- Principle: voltage-controlled resistance
- Architecture: power transistor, sense resistor, reference voltage, error amplifier
- Dropout voltage (~100 mV)
- DC metrics: power efficiency, current efficiency, line regulation, load regulation
- Error amplifier specs: gain, slew rate, PSR
- Transient response: step changes in input voltage and load current

#### Linear Regulators – Advanced Topics

- Voltage-mode vs. current-mode control
- PMOS vs. NMOS power devices
- Stability analysis: poles/zeros, Miller compensation, zero-canceling resistor
- Slew-rate enhancement & dynamic biasing
- Noise & power-supply rejection considerations
- Over-charge protection, capacitor-less LDO designs

#### Protection & Reference Circuits

- Overvoltage, undervoltage, and overtemperature protection
- Bandgap voltage & current references
- Start-up circuits and power-on-reset
- Short-circuit and over-current protection

#### Switching Regulators – Fundamentals

- Comparison of switching vs. linear regulation
- Converter topologies: LC vs. capacitive-only
- Synchronous vs. non-synchronous DC/DC
- Voltage-mode vs. current-mode, Buck vs. Boost, PFM vs. PWM, CCM vs. DCM
- Inductive vs. inductorless operation
- Stability considerations

### LC Buck Converter

- Inductor sizing & current ripple
- Schematic & operating principle
- Line & load regulation
- Efficiency, stability, noise & PSRR analysis
- Compensator design (Type I/II/III)

### LC Boost Converter

- Inductor sizing & current ripple
- Schematic & operating principle
- Line & load regulation
- Efficiency, stability, noise & PSRR analysis
- Comparison to Buck topology

### Capacitive Buck Converters (SCVR)

- Series-parallel topologies (Dickson, ladder, Fibonacci)
- Equivalent output resistance
- Flying-capacitor and switch sizing
- Efficiency and regulation methods

### Capacitive Boost Converters (Charge Pumps)

- Diode-based vs. transistor-based charge pumps
- Stage cascading & closed-loop control

### Near-Field Wireless Power Transfer

- Principles: electromagnetic vs. electrostatic induction
- Basic architectures & operating frequencies
- Near-field vs. far-field applications

### Far-Field Wireless Power Transfer & RF Energy Harvesting

- RF energy harvesting for low-power IoT: impedance matching, rectification, MPPT
- RF path loss and power budgeting
- Full chain: RFEH → Boost → MPPT → Buck → LDO
- Far-field application examples

### **Intended Learning Outcomes:**

Upon successful completion of the module, students will be able to:

Understand fundamental PMIC concepts and architectures:

Grasp the operating principles and block-level structures of power management ICs, including low-dropout regulators (LDOs), switching converters, charge pumps, power sequencing and protection circuits.

Connect theoretical models to real-world behavior:

Develop insight into how small-signal and large-signal models predict regulator dynamics, stability margins and transient response, and relate these models to measured circuit performance.

Describe the interplay between specifications, sizing and topology:

Explain how key requirements—output accuracy, load/regulation transients, efficiency and noise—drive choices in transistor sizing, passive component selection (inductors, capacitors) and overall PMIC topology.

**Teaching and Learning Methods:**

Throughout the semester, core power-management IC principles and theoretical frameworks are introduced in weekly lectures. Each week, students will receive self-study exercises—drawn from the lecture materials and selected reference papers—to deepen their understanding. These exercises are then reviewed and discussed in dedicated problem-solving sessions with Q&A. In addition, students are expected to engage in independent study of the provided lecture notes, tutorials and research articles to fully master the course content.

**Media:**

MS PowerPoint Slides, Moodle, LTspice, Matlab

**Reading List:**

Wicht, Bernhard. Design of Power Management Integrated Circuits. John Wiley & Sons, 2024.  
Hu, John, and Mohammed Ismail. CMOS high efficiency on-chip power management. Springer Science & Business Media, 2011.

**Responsible for Module:**

Brederlow, Ralf; Prof. Dr.-Ing.

**Courses (Type of course, Weekly hours per semester), Instructor:**

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### EI70520: Circuit Design for Security | Circuit Design for Security [CDS]

Version of module description: Gültig ab summerterm 2025

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> summer semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 75	<b>Contact Hours:</b> 75

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

Knowledge and theoretical understanding of basic elements of digital circuits and of typical circuit design problems, as well as the ability to select solutions for typical circuit design problems, particularly in the context of security, will be examined in the form of open and closed questions in a written exam (60 minutes). The questions are to be answered without additional documents and in the form of short text or bullet points. Calculations may be necessary to answer the questions. The practical skills to independently implement, synthesize, and simulate essential elements of digital circuits are demonstrated by solving 3-5 implementation tasks. A grade bonus of 0.3 is awarded to the final grade for the successful completion of all tasks. The practical tasks are a voluntary mid-term assignment.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Basic knowledge in VHDL

Basic knowledge of IT security as taught, e.g., in the lectures Grundlagen der IT-Sicherheit and Angewandte Kryptographie

#### Content:

In this module, the development of digital circuits in the security context is examined starting from basic circuits. First of all, the knowledge of implementing state machines will be refreshed and extended. The implementation of important components of digital circuit design such as FIFOs and LFSRs is introduced. The implementation of pseudo-random number generators based on LFSRs and their application in the security context will be discussed. The implementation of multipliers is essential in many cryptographic applications. For this purpose, fundamental implementations as well as special variants for modulo-multiplication are discussed in the module. Also, concepts are

discussed to test cryptographic circuits appropriately; Implementation strategies are introduced to optimize circuits in terms of area, power consumption, and performance.

In addition to the theoretical teaching of the content in lectures, the practical relevance is clarified in exercises and in a lab course. The students also learn to implement and synthesize digital circuits with a commercial design tool.

### **Intended Learning Outcomes:**

After successful completion of the module, students have the following qualifications:

- They know essential elements of digital circuits such as state machines, FIFOs, LFSRs and multipliers and can implement them independently.
- They know typical circuit design issues such as clock domain crossing, the choice of synchronous and asynchronous reset or the testability of circuits and can choose suitable solutions.
- They know application scenarios of multipliers and LFSRs in the security context, can understand the theoretical foundations of the concepts discussed, and can name the advantages and disadvantages of these.
- They are able to describe digital circuits in VHDL and perform initial synthesis steps.

### **Teaching and Learning Methods:**

Lecture and exercise content is provided through slides and blackboard. The learning process of students is supported in the exercises by interactively solving tasks, group work and program demonstrations of the advisor which show implementation tasks and security scenarios.

Programming exercises during the semester give students the opportunity to practice and to demonstrate their skills in implementing and synthesizing digital circuits in a security context using a commercial design tool.

### **Media:**

In lecture and exercise, slides, blackboard, example code and interactive online tools, e.g. Question Catalogs, are used. The offer is complemented by a forum on Moodle, where teachers answer questions about the content and the lab course tasks.

### **Reading List:**

Niklaus Wirth; Digital Circuit Design for Computer Science Students - An Introductory Textbook; Springer; 1995 ISBN 978-3-540-58577-0

Further literature recommendations will be provided at the beginning of each semester through the Moodle course.

### **Responsible for Module:**

Pehl, Michael, Dr.-Ing. habil.: m.pehl@tum.de

### **Courses (Type of course, Weekly hours per semester), Instructor:**

Circuit Design for Security (Forschungspraktikum, 1 SWS)

Pehl M ( Stein N )

Circuit Design for Security (Übung, 2 SWS)

Pehl M ( Stein N )

Circuit Design for Security (Vorlesung, 2 SWS)

Pehl M ( Stein N )

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### EI71013: System Design for the Internet of Things | System Design for the Internet of Things [SDIOT]

Version of module description: Gültig ab summerterm 2017

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> summer semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 90	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

Achievement of the intended learning outcomes is assessed in a single written exam (75 min) at the end of the semester. The written exam is performed in a closed book policy without supporting material.

Assessment criteria are:

Ability to make design decisions for an IoT system architecture regarding algorithms, protocols, platforms and methodologies which have been discussed in the course, combining theoretical concepts with practical implementation considerations.

Ability to apply methods, concepts and algorithms to solve system design problems in an IoT system design context.

Ability to combine approaches from the sensing, computation and communication domain for IoT device design.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Basic principles of embedded systems, internet communication, programming.

#### Content:

Introduction to embedded and cyber-physical systems and the IoT; application scenarios for IoT; wireless sensor networks and IoT; design and modeling of embedded platforms; sensors, actuators and computation/control; processing of large data sets; energy supply and constraints; architectures of distributed systems; Internet principles; communication frameworks and protocols; consumer-producer and publisher-subscriber communication patterns; safety, information security and privacy concepts; software design patterns for dependable systems; system simulation and

validation; application examples, among others, from the smart energy, smart manufacturing and automotive domains.

**Intended Learning Outcomes:**

Upon successful completion of the module, the participants are able to make informed design decisions for the development of Internet of Things (IoT) devices and applications. They will be able to evaluate, compare and apply different platforms, algorithms, protocols and system architectures for IoT applications, considering sensing, computation, communication and energy aspects. They will be able to apply the learned design methodologies, algorithms and protocols to develop new applications based on examples from, e.g., the smart energy domain which are presented in the course. Critical reflection on the societal impact of the IoT together with safety, security and privacy aspects will be encouraged.

**Teaching and Learning Methods:**

In addition to the students' individual methods which shall be supported by the lectures, the tutorials will repeat and deepen the course content by discussion of problems and exercises in form of learning activities.

During the lectures, students are instructed in a teacher-centered style, integrating interactive components. The exercises are held in a student-centered way, encouraging learning activities and providing formative feedback.

**Media:**

- Presentations (Projector, Blackboard)
- E-learning platform Moodle
- Exercises with solutions available for download

**Reading List:**

- McEwen, Adrian, and Hakim Cassimally. Designing the internet of things. John Wiley & Sons, 2013.
- Vermesan, Ovidiu, and Peter Friess, eds. Internet of things - from research and innovation to market deployment. River Publishers, 2014.
- Lee, Edward Ashford, and Sanjit Arunkumar Seshia. Introduction to embedded systems: A cyber-physical systems approach. Lee & Seshia, 2011.

Further literature will be discussed in the lecture.

**Responsible for Module:**

Steinhorst, Sebastian; Prof. Dr.

**Courses (Type of course, Weekly hours per semester), Instructor:**

System Design for the Internet of Things (Vorlesung mit integrierten Übungen, 4 SWS)

Steinhorst S, Calipari M, Debnath R, Binkert R, Lüdecke M, Hamad M

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### EI71029: Physical Unclonable Functions | Physical Unclonable Functions [PUFs]

Version of module description: Gültig ab winterterm 2025/26

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 75	<b>Contact Hours:</b> 75

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The achievement of the learning objectives of the module is demonstrated in the form of a 60-minute written examination. Students demonstrate that they can name and explain concepts and applications for PUFs and TRNGs, including the post-processing of the raw data obtained from them. They demonstrate their knowledge of the PUF and TRNG structures discussed by creating and explaining schematic representations. By interpreting the results of methods for quality assessment of PUFs and TRNGs, explaining how these methods are used and where possible weaknesses of the methods lie, they demonstrate their understanding and ability to apply such methods and show that they can critically question the results of the assessment procedures. They demonstrate their knowledge and understanding of typical attack vectors on PUFs by naming and explaining them; by naming and discussing suitable countermeasures and explaining them in detail, students demonstrate their knowledge and ability to select suitable countermeasures. If the number of participants is low, the examination can be converted into a 30-minute oral examination.

**Practical Assignment:** Students demonstrate that they are able to practically implement selected concepts for PUFs discussed in the lecture on an FPGA by means of the practical part of the course, which consists of three to four subtasks and represents a voluntary mid-term performance. A grade bonus of 0.3 is awarded for the successful completion of subtasks, which is voluntary in the style of a mid-term assignment.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Prior knowledge of VHDL is required to complete the lab.

No special preknowledge is required for the lecture.

**Content:**

This lecture addresses concrete concepts to utilize randomness which is available in hardware for IT-security. In the first part of the lecture, Physical Unclonable Functions (PUFs) are considered. First, concepts of PUFs are presented on a circuit level and effects, which are used, are discussed. Next, metrics for quality evaluation of PUFs are taught and applications of PUFs are presented. Required components for applications of PUFs are discussed as well as attacks and countermeasures. In a second part of the lecture, true random number generators (TRNGs) and methods to analyze TRNGs are addressed.

In the lab part of the project, students implement on their own a module for en- and decryption of data on FPGA using a PUF. The goal is to implement key storage and random number generation on an FPGA where interface specification must be met. Modules for en- and decryption as well as for communication are provided.

The exercise part of the module is dedicated to practice the content of the lecture, on the one hand. On the other hand, it helps the students in transferring content from the lecture to the lab part and supports the lab part.

**Intended Learning Outcomes:**

After successful completion of the module, students know the concepts of Physical Unclonable Functions and random number generators. They can apply and interpret metrics for quality evaluation of PUFs and random numbers. Students know and understand applications of PUFs. They can apply their knowledge on PUFs and random number generators and can use to implement basic PUF applications.

**Teaching and Learning Methods:**

Teacher-centered teaching is used in the lecture of this module to provide knowledge regarding concepts of PUFs and RNGs, evaluation methods for PUFs, and application of PUFs. The understanding of these theoretical contents is advanced in an exercise where interactive teacher-centered teaching is used as a learning method. Furthermore, in the exercise, knowledge regarding the transfer from theory into practice is provided.

Also, students learn important aspects of practical implementations of PUFs and RNGs in the laboratory part of the module. Theoretical background for the laboratory part is provided in the lecture. The knowledge on how to transfer theory into practice is taught in the exercise. Based on that, students have to find solutions for the realization of typical components of PUF applications on their own. The components which are to be implemented are specified. Literature resources as well as discussions with a supervisor can be used to solve the task.

**Media:**

- Lecture/Exercise: PowerPoint and blackboard presentation
- Lab: Brief instruction

**Reading List:**

The following literature is recommended:

- C. Böhm und M. Hofer, "Physical Unclonable Functions in Theory and Practice", Springer 2012
- M. Hiller, "Key Derivation with Physical Unclonable Functions ", Dissertation, TUM 2016
- J. Delvaux, "Security Analysis of PUF-Based Key Generation and Entity Authentication", PhD Thesis, KU Leuven, 2017
- M. Pehl, "Design, Evaluation, and Application of Security Primitives that are Based on Hardware-Intrinsic Features", Cummulative Habilitation Thesis, TUM, 2024

**Responsible for Module:**

Sigl, Georg; Prof. Dr.-Ing.

**Courses (Type of course, Weekly hours per semester), Instructor:**

Physical Unclonable Functions (Vorlesung mit integrierten Übungen, 3 SWS)

Pehl M

Physical Unclonable Functions (Praktikum, 2 SWS)

Pehl M

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### EI71036: Software Architecture for Distributed Embedded Systems | Software Architecture for Distributed Embedded Systems [SADES]

Version of module description: Gültig ab winterterm 2022/23

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 105	<b>Contact Hours:</b> 45

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

Achievement of the intended learning outcomes is assessed in a single written exam (75 min) at the end of the semester. The written exam is performed in a closed book policy without supporting material.

Assessment criteria are:

Ability to make design decisions for software architecture based on design patterns which have been discussed in the course, combining theoretical concepts with practical implementation considerations.

Ability to apply methods, concepts and design patterns related to software architecture for embedded and distributed systems.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Principles of embedded computing systems, object oriented programming.

#### Content:

Introduction to object oriented software development; Unified Markup Language (UML) representation; basic principles of pattern-oriented software design; specific requirements for embedded systems; challenges of distributed architectures; selected structural, behavioral and creational "gang of four" design patterns which are relevant to the targeted applications; design patterns in the context of resource constrained embedded systems: hardware access, concurrency and resource management, safety and reliability; patterns for event handling, service access, configuration and concurrency of distributed applications.

**Intended Learning Outcomes:**

Upon successful completion of the module, the participants are able to explain, apply and develop software architectures for embedded and distributed systems. The students are able to discuss and evaluate different architectural design patterns and design paradigms for such systems. They are able use the learned methods for both the choice of appropriate software architectures and to solve specific problems for applications based on the insights provided in this course, as well as to apply the methods and architectural concepts in system design processes.

**Teaching and Learning Methods:**

In addition to the students' individual methods which shall be supported by the lectures, the tutorials will repeat and deepen the course content by discussion of problems and exercises in form of learning activities.

During the lectures, students are instructed in a teacher-centered style, integrating interactive components. The exercises are held in a student-centered way, encouraging learning activities and providing formative feedback.

**Media:**

The following media are used:

- Presentations (Projector, Blackboard)
- E-learning platform Moodle
- Exercises with solutions available for download

**Reading List:**

- Pattern-Oriented Software Architecture, Patterns for Concurrent and Networked Objects, Volume 2, by Douglas Schmidt, Michael Stal, Hans Rohnert and Frank Buschmann
- Design Patterns: Elements of Reusable Object-Oriented Software, Book by Erich Gamma, John Vlissides, Ralph Johnson, and Richard Helm

Further literature will be discussed in the lecture.

**Responsible for Module:**

Steinhorst, Sebastian; Prof. Dr.

**Courses (Type of course, Weekly hours per semester), Instructor:**

Software Architecture for Distributed Embedded Systems (Vorlesung mit integrierten Übungen, 3 SWS)

Steinhorst S, Demicoli J, Calipari M, Debnath R, Hamad M

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### EI71059: Mixed Integer Programming and Graph Algorithms for Engineering Problems | Mixed Integer Programming and Graph Algorithms for Engineering Problems [MIPGA]

Version of module description: Gültig ab winterterm 2025/26

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> summer semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 90	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The examination will be in written form, the duration is 75 minutes.

The students will demonstrate their capability to construct abstract models for commonly-seen engineering problems at given examples. They will show that they can select and apply appropriate solution algorithms and derive the corresponding mathematical constraints and objectives. They will also show that they can analyze the algorithm efficiency as well as the result quality.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Fundamental programming knowledge

#### Content:

Content covered in this course:

- Physical modeling, mixed integer linear programming (MILP), time complexity
- Graph: vertex, edge, directed, degree, cyclic, planarity
- Tree: binary search tree, MILP sort, quick sort, heaps
- Distance-oriented graph: MILP shortest path, Dijkstra, A\*, MILP spanning tree, Kruskal, MILP steiner tree, MILP planar routing
- Conflict-oriented graph: vertex coloring, edge coloring, maximum independent set
- Graph partition: max-flow min-cut, clustering
- Set: set covering, exact covering
- Scheduling and binding: time slot modeling, non-uniform time slot

**Intended Learning Outcomes:**

After accomplishing this module, students are able to construct abstract models (e.g. graphs) for commonly-seen engineering problems, and apply algorithms or mathematical modeling methods to solve the problems systematically.

In particular, students are able to analyze the problem space and solution space for a given engineering problem and understand that a small variance of the problem formulation can cause a significant change to the methodology. In addition, with a given method, students are able to evaluate its time complexity and measure its solution quality.

**Teaching and Learning Methods:**

Students learn the content of this course by attending the lectures and the tutorials. While the lectures focus on teaching the theories, the tutorials focus on consolidating students' knowledge by applying learnt models and methods to solve varying problems.

Both the lectures and tutorials are held in a teacher-centered style, but the students are always encouraged to interact with the lecturer and the tutor, especially when the students have different ideas regarding the models or algorithms.

**Media:**

The following kinds of media are used:

- Slides
- Blackboard presentations
- Online examples and demos

**Reading List:**

The following literatures are recommended:

- Applied Mathematical Programming; Bradley, Hax, and Magnanti; Addison-Wesley 1977.
- Introduction to Algorithms; Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest, and Clifford Stein; The MIT Press 2009.
- Introduction to Graph Theory; Douglas B. West; Pearson 2000.

**Responsible for Module:**

Schlichtmann, Ulf; Prof. Dr.-Ing.

**Courses (Type of course, Weekly hours per semester), Instructor:**

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### EI71070: Advanced Cryptographic Implementations | Advanced Cryptographic Implementations [ACIm]

Version of module description: Gültig ab summerterm 2025

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> summer semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 105	<b>Contact Hours:</b> 45

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The examination consists of a 60-minute written exam. In this examination, the understanding of the knowledge imparted in the lecture on the implementation of symmetric cryptographic procedures and hash functions, on the implementation of asymmetric cryptographic procedures as well as on the optimization and hardening of cryptographic procedures against implementation attacks is demonstrated by answering open and closed questions.

If the number of participants is low, the examination can be held in oral form.

Translated with DeepL.com (free version)

#### Repeat Examination:

Next semester / End of Semester

#### (Recommended) Prerequisites:

The following lectures should be successfully completed: Applied Cryptography or equivalent. Further, the following courses are recommended: "Secure implementations of cryptographic devices", "SmartCard Lab", and "Seminar on Security in Information Technology".

#### Content:

This module introduces methods and techniques to securely and efficiently implement state-of-the-art cryptographic algorithms on embedded systems, including countermeasures against physical attacks such as side-channel and fault attacks.

The module is organized into the following thematic blocks:

- Secure implementation of symmetric cryptographic algorithms, e.g., AES-GCM and ChaCha20-Poly1305.

- Efficient implementation of asymmetric cryptographic algorithms incl. post-quantum cryptography, e.g., Kyber and Dilithium.
- Special topics: Discussion of current research results.

As part of the thematic blocks, students will be required to implement cryptographic algorithms and prepare presentations on current research work as homework assignments.

**Intended Learning Outcomes:**

Upon successful completion of the module, students will master advanced implementation techniques to optimize state-of-the-art cryptographic algorithms for embedded systems. Additionally, students will be able to implement advanced countermeasures to secure cryptographic implementations against implementation attacks such as side-channel and fault attacks.

**Teaching and Learning Methods:**

The module is offered as lectures using slides and notes on the blackboard. In the lectures, the contents will be provided in a talk with practical examples and demonstrations, as well as through discussion with the students. In each lecture, further literature will be suggested to motivate students to deepen their understanding of the methods and concepts presented in the lecture. During the exercise sessions students will be invited to present current research results assigned as homework during the course. Discussions will be held to consolidate the shared understanding to the class.

**Media:**

Presentation slides, blackboard, and research papers.

**Reading List:**

The following textbooks are recommended:

1. Cetin Kaya Koc, Cryptographic Engineering, Springer Verlag, 2009
2. Joseph Yiu, The Definitive Guide to ARM® Cortex®-M3 and Cortex®-M4 Processors. 2013
3. Stefan Mangard, Elisabeth Oswald, Thomas Popp: Power Analysis Attacks Revealing the Secrets of Smart Cards, Springer Verlag, 2007

Further readings will be suggested during the course.

**Responsible for Module:**

Sigl, Georg; Prof. Dr.-Ing.

**Courses (Type of course, Weekly hours per semester), Instructor:**

Advanced Cryptographic Implementations (Vorlesung mit integrierten Übungen, 3 SWS)

De Santis F ( Budak U )

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### EI71073: Quantum Computers and Quantum Secure Communications | Quantum Computers and Quantum Secure Communications [QSCoM]

*Quantum Computers and Quantum Secure Communications*

Version of module description: Gültig ab summerterm 2025

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> summer semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 90	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The evaluation is individual. The capabilities to: i) understand the main concepts for quantum computers and post-quantum cryptography; ii) be familiar with the quantum and post-quantum algorithms; and iii) understand the vulnerabilities of post-quantum cryptographic implementations are evaluated through a written exam (60 minutes) (oral examination if the number of students is low).

In addition, the capabilities to: i) evaluate the security and performance of Post-Quantum cryptographic implementations; and 5) apply security countermeasures to post-quantum cryptographic implementations are evaluated through practical exercises and a project task. Passing those exercises and project is rewarded with a bonus of 0.3 towards the final grade. The exercises are a voluntary mid-term performance.

#### Repeat Examination:

End of Semester

#### (Recommended) Prerequisites:

Good knowledge of Microcontroller programming, basics on security like it is taught in the lecture Embedded Systems and Security.

#### Content:

The course is comprised of a lecture accompanied by exercises and a project part.

The topics presented in the class are:

- 1) Introductory lecture;
- 2) Quantum computing and technologies;
- 3) Quantum algorithms;

- 4) Post-quantum algorithms general description;
- 5) Post-quantum implementation and evaluation;
- 6) Secure implementation.

**Intended Learning Outcomes:**

At the end of this module, students 1) are able to understand the basic concepts of quantum computers and post-quantum cryptography; 2) are familiar with quantum and post-quantum algorithms; 3) understand the vulnerabilities of post-quantum cryptography implementations; 4) can evaluate the security and performance of Post-Quantum cryptographic implementations; and 5) can apply security countermeasures to post-quantum cryptographic implementations.

**Teaching and Learning Methods:**

Individual support by the advisor, introductory lectures, examples and support for the seminar exercises are given.

In addition, the following methods are used: i) Real use cases of the presented concepts; ii) invited talks from industry partners; iii) Videos; iv) in-class discussions and presentations; v) exercises and experience sharing.

**Media:**

board, slides and articles

**Reading List:**

Post-Quantum Cryptography. Daniel J. Bernstein, Johannes Buchmann, Erik Dahmen, 2009. Springer-Verlag Berlin Heidelberg.

Post-Quantum Cryptography: Code-Based Cryptography and Hash Based Signatures Schemes, Umaa, Valrie Gauthier, 2014, isbn 3639715500. Scholar's Press.

NIST Post-Quantum Submissions <https://csrc.nist.gov/projects/post-quantum-cryptography/round-2-submissions>

**Responsible for Module:**

Sigl, Georg; Prof. Dr.-Ing.

**Courses (Type of course, Weekly hours per semester), Instructor:**

Quantum Computers and Quantum Secure Communications (Praktikum, 1 SWS)  
Sepulveda Florez M ( Pehl M )

Quantum Computers and Quantum Secure Communications (Vorlesung mit integrierten Übungen, 3 SWS)

Sepulveda Florez M ( Pehl M )

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### **EI71095: Multi-criteria Optimization and Decision Analysis for Embedded Systems Design | Multi-criteria Optimization and Decision Analysis for Embedded Systems Design [MCODA]**

*Introduction to multi-objective optimization and multi-criteria decision analysis*

Version of module description: Gültig ab winterterm 2021/22

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 120	<b>Contact Hours:</b> 30

Number of credits may vary according to degree program. Please see Transcript of Records.

#### **Description of Examination Method:**

Written examination (60 minutes):

The students will be examined through a written examination where they prove that they have understood the application of the multi-criteria paradigm and can apply it to perform analysis, modeling, optimization, and decision making for problems encountered in embedded systems design. The questions will cover the theoretical background presented during the lectures as well as exercises from the lecture. The examination lasts 60 minutes and will be carried out without helping material.

Exercise assignment:

As part of the self-study time, an exercise assignment (homework) in groups of 2-3 participants will be assessed, where the students have to demonstrate that they can solve real world optimization problems coming from a current research area. Given the size of such problems this cannot be covered in the written exam. The assessment process of this part will be carried out through deliverables and a report.

The final grade is the weighted average of the written examination (60%) and the exercise assignment (40%).

#### **Repeat Examination:**

Next semester

#### **(Recommended) Prerequisites:**

- Data structures
- Basic programming skills in Python or Matlab; alternatively C/C++ or Java

- Basic knowledge of probability and statistics (probability axioms and theorems, e.g. Bayes' Theorem and its applications; typical probability distributions, e.g. exponential, Gaussian, etc.)

**Content:**

1. Introduction to the multi-criteria paradigm for embedded systems design
  - Uni-criterion vs multi-criteria
  - Modeling and challenges
2. Optimization methods
  - Linear programming
  - Metaheuristics (e.g. genetic algorithms, simulated annealing)
  - Multi-objective optimization for design space exploration
3. Decision making processes
  - Voting theory
  - Multi-criteria decision analysis
  - Game theory
  - Decision under risk and uncertainty

During the lecture, the theoretical content will be accompanied by examples illustrating the following concepts: problem abstraction and modeling, algorithm selection and implementation, multi-criteria decision making and analysis. Thereby both functional and non-functional aspects will be considered. More elaborate exercises on these topics will be done in self-study by the students.

**Intended Learning Outcomes:**

Upon successful completion of this module, students are able to:

- understand the multi-criteria paradigm and its challenges for embedded systems design,
- analyze and model encountered problems with this paradigm,
- understand how different (multi-objective) optimization methods work, select and apply the most suitable one(s) depending on the situation,
- understand how different (multi-criteria) decision making methods work, select and apply the most suitable one(s), as well as analyze the results obtained after the optimization process.

**Teaching and Learning Methods:**

The technical content will be introduced by means of lectures with PowerPoint presentations and will be illustrated with small examples that will be included in the slides. The students are encouraged to ask questions. In addition to the individual learning methods of the students, the transfer of the theoretical knowledge to its practical application will be achieved through illustrative examples during the lectures and additional exercises to be done in self study manner. All the course material will be made available to the students through Moodle.

**Media:**

The following media forms are used:

- Presentations with handwritten annotations
- Description of illustrative examples and exercises

**Reading List:**

Optional literature recommendations:

- X.S. Yangi, "Engineering Optimization: An Introduction with Metaheuristic Applications", Wiley 2010
- EG. Talbi, "Metaheuristics: From Design to Implementation", Wiley 2009
- S. Greco, M. Ehrgott, J.R. Figueira (Eds.), "Multiple Criteria Decision Analysis: State of the Art Surveys", Springer 2016

**Responsible for Module:**

Herkersdorf, Andreas; Prof. Dr.

**Courses (Type of course, Weekly hours per semester), Instructor:**

Multi-Criteria Optimization and Decision Analysis for Embedded Systems Design (Vorlesung, 2 SWS)

Doan N

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### EI71104: Embedded System Design for Machine Learning | Embedded System Design for Machine Learning [Embedded ML]

Version of module description: Gültig ab summerterm 2024

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 6	<b>Total Hours:</b> 180	<b>Self-study Hours:</b> 90	<b>Contact Hours:</b> 90

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

- 1) Code submission for the lab part (coursework, 20% of final grade)
- 2) Written final exam (90min) (Examination, 80% of final grade)

1) The student will hand in code submissions for the three lab parts, which will be graded. This grade counts 20% of the final grade.

2) In the final exam (90min written or 30min oral), the students will answer questions from the lecture content and from the lab part to test their understanding of the theoretical and practical aspects of embedded machine learning. This grade counts 80% of the final grade.

The first part (1) will test that the students have acquired the practical programming skills to deploy a ML embedded project, while part (2) tests for the understanding of the practical and theoretical concepts of embedded ML.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Basic knowledge on embedded C and micro-controllers (e.g. in the form of a micro-controller programming lab) is assumed to be known.

Basic knowledge of Hardware design in VHDL or Verilog (e.g. in the form of a hardware design lab or the lecture "Entwurf Digitaler Systeme mit VHDL und SystemC" (Prof. Ecker) is assumed to be known.

Basic knowledge of machine learning algorithms (e.g. in the form of the computational intelligence lecture or the lecture Machine Learning: Methods and Tools lecture) is recommended.

**Content:**

The lecture will cover the following contents:

\* Introduction to the design flow and design steps to deploy machine learning workloads on embedded devices

\*

Machine learning theory to understand the typical structure, operators and trade-offs in accuracy, memory and performance demands of machine learning workloads

\* Neural Network Model Compression Methods: Number systems, Integer and sub-byte Quantization, Quantization-aware training, Pruning, Rank Reduction.

\* Software Optimization Methods: Memory planning, target-aware operator optimization, operator fusing and tiling

\* Methods and basic HW blocks for embedded HW-acceleration (SIMD, Vector Instructions, loosely-coupled accelerators, memory systems)

The lab part will cover the following contents to transfer the theory into practice:

\* Introduction to the Machine Learning Deployment Toolchain TVM

\* Training, model optimization and deployment of a keyword recognition application onto a low-power micro-controller board using TVM

\* Design of a simple HW accelerator to offload machine learning workload into hardware with test by simulation.

**Intended Learning Outcomes:**

Upon completion of this module, students are able to:

\* Understand the design flow and design steps for deploying machine learning workloads on embedded devices.

\* Evaluate the trade-offs involved in executing machine learning workloads such as neural network inference in software and hardware for on embedded processors and dedicated accelerators.

\* Apply effectively model compression methods to embedded machine learning workloads and understand the theory behind the methods.

\* Apply hardware acceleration principles (SIMD, Vector, 2D systolic arrays) for accelerating ML workloads and know about the influence of the memory system.

\* Apply a state-of-the-art machine learning deployment flow to a simple machine learning application such as keyword recognition.

\* Implement the deployment code on an embedded processor platform (micro-controller board) and to design a simple hardware accelerator for the application that works in simulation.

### **Teaching and Learning Methods:**

The module will consist of two parts, a weekly lecture and a parallel lab with three parts.

The lecture will consist of classroom sessions with slide presentation. The exercises will be integrated in the lecture flow in order to apply the learned content directly on example problems. This will be done using activating methods such as group works.

The lab will be split into three major tasks, that will be tutored, each being introduced in one classroom lab session. The students will work on these tasks in small groups on their own schedule to also train team work and independent work. The lab tasks will directly put the lecture content into practise, hence, following a problem-oriented learning approach.

### **Media:**

The course will be taught based on lecture material in the forms of slides and with additional exercises. The lab part will involve the work on a state of the art open-source simulation and deployment flow (TVM) that can be used either on university lab PCs or private machines. Additionally, low-power micro-controller boards will be used to demonstrate the application in real hardware.

### **Reading List:**

There exist textbooks covering the content of the lectures so far. Following books cover parts of the lecture's content and provide related information:

\* Vivienne Sze, Yu-Hsin Chen, Tien-Ju Yang, Joel S. Emer; Efficient Pro-cessing of Deep Neural Networks; Morgan & Claypool Publishers

\* David Patterson, John Hennessy; Computer Organization and Design RISC-V Edition - The Hardware Software Interface; Elsevier

### **Responsible for Module:**

Schlichtmann, Ulf; Prof. Dr.-Ing.

### **Courses (Type of course, Weekly hours per semester), Instructor:**

Embedded System Design for Machine Learning (Praktikum, 3 SWS)  
Ahmadifarsani S, van Kempen P, Ecker W, Schlichtmann U, Fengler P

Embedded System Design for Machine Learning (Vorlesung mit integrierten Übungen, 3 SWS)  
Ecker W, van Kempen P, Ahmadifarsani S, Schlichtmann U

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### EI71108: CMOS Analog-to-Digital Converters | CMOS Analog-to-Digital Converters [ADC]

Version of module description: Gültig ab summerterm 2022

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> summer semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 90	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The assessment consists of a written final exam (60 minutes), in which students demonstrate their understanding of the fundamental concepts and architectures of CMOS-based digital-to-analog and analog-to-digital converters, as well as their ability to apply this knowledge to practical design tasks.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Solid-State and Semiconductor Device Physics,  
Analog and Mixed-Signal Electronics.

#### Content:

1. Fundamentals of discrete-time signal processing
2. Fundamentals of CMOS technology
3. Sample & hold circuits
4. Switched-capacitor circuits
5. Data converter fundamentals
6. Nyquist-rate D/A converters
7. Nyquist-rate A/D converters
8. Sigma-Delta A/D converters

#### Intended Learning Outcomes:

Upon successful completion of the module, students are able to understand the concepts and architectures of CMOS-based digital-to-analog and analog-to-digital converters. They have insight

into typical non-idealities of such circuits and are able to describe the fundamental relationships between circuit specifications, device sizing, and circuit architecture.

**Teaching and Learning Methods:**

Weekly lecture (2 hours per week) focusing on the presentation of theoretical concepts and foundations.

Weekly exercise session (2 hours per week) where these concepts are applied in practical and theoretical tasks.

**Media:**

Presentation slides, Moodle forum for discussions and announcements, exercise sheets with sample solutions, lecture notes and solutions from the tutorials.

**Reading List:**

F. Maloberti, Data Converters,

T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design.

**Responsible for Module:**

Brederlow, Ralf; Prof. Dr.-Ing.

**Courses (Type of course, Weekly hours per semester), Instructor:**

CMOS Analog-to-Digital Converters (Vorlesung mit integrierten Übungen, 4 SWS)

Burcea F, Jankowski M, David K, Brederlow R

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### EI7271: Chip Multicore Processors | Chip Multicore Processors [CMP]

Version of module description: Gültig ab summerterm 2023

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> summer semester
<b>Credits:*</b> 6	<b>Total Hours:</b> 180	<b>Self-study Hours:</b> 135	<b>Contact Hours:</b> 45

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The exam (written, 75 minutes) is adjusted to the different topics conveyed. Thereby, the students should proof their knowledge in problems and approaches for parallel processing in chip multicore processors. For this, they have to answer questions and solve given problem cases.

The final grade is made up exclusively by the final exam.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Basic understanding of computer architectures. Ideally: 'System-on-Chip Technologies' lecture.

#### Content:

The lecture starts with the motivation for chip multicore processors. Starting from the technological background, the potential and challenges of parallel execution are discussed and state-of-the-art processors will be presented to classify multicore processors. A central aspect of chip multicore processors is the memory hierarchy. With the introduction of caches the coherency problem arises. Solutions for this problem are discussed during the lecture. The implementation of synchronization, both from the hardware and the software view, are discussed subsequently. Non-blocking data structures and Transactional Memory are introduced as possible solutions to relax the synchronization problem. The on-chip interconnect, and especially Network-on-Chip (NoC) are discussed in detail as part of the lecture. Finally, programming models and implementation challenges are discussed.

#### Intended Learning Outcomes:

After completion of the course the students know the basics of problems and approaches of parallel execution with chip multicore processors.

They are able to discuss relevant problems and state-of-the-art processor example on concept level. Students know how to classify processor architectures with respect to their characteristics.

**Teaching and Learning Methods:**

The basic learning method is presentation during the lecture, supplemented with group discussions. During the tutorial examples will be discussed. For a better understanding students will read scientific publications as self studies. Case studies will be discussed to get a practical understanding of chip multicore processors.

**Media:**

The following types of media are used:

- Presentation with notebook and projector
- lecture notes
- scientific publications

**Reading List:**

John L. Hennessy und David A. Patterson, Computer Architecture - A Quantitative Approach, Academic Press, 4. Edition

Maurice Herlihy und Nir Shavit, The Art of Multiprocessor Programming, Morgan Kaufmann, 1. Edition

David E. Culler, J. P. Singh und Anoop Gupta, Parallel Computer Architecture: A Hardware/ Software Approach, Morgan Kaufmann, 1. Edition

**Responsible for Module:**

Herkersdorf, Andreas; Prof. Dr.

**Courses (Type of course, Weekly hours per semester), Instructor:**

Chip Multicore Processors (Vorlesung mit integrierten Übungen, 3 SWS)

Liess M [L], Herkersdorf A, Wild T, Twardzik T

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### EI7355: Nanosystems | Nanosystems [NanoSys]

Version of module description: Gültig ab winterterm 2024/25

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter/summer semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 90	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The examination consists of a written exam (60 minutes, 100%). In the written exam, students will demonstrate theoretical knowledge of applied methods of nanosystems, nanodevices, and nanometrology techniques by answering questions under time constraints and without aids. Students will demonstrate the ability to explain fundamental concepts of nanosystems in a condensed form using sketches and block diagrams of instrumentation, measurement and fabrication setups.

In the laboratory part offered to accompany the lecture, the emphasis is on hands-on training of students in a real metrology laboratory environment. The voluntary examination performance for this includes a measurement report (2 pages), which demonstrates that the students have deepened their knowledge from the practical laboratory and have acquired a comprehensive understanding of the measuring instruments and the devices under investigation. The students show that they can use analysis tools and visualization programs to check the results they have obtained themselves.

A grade bonus of 0.3 will be applied to the final grade for successful completion of the voluntary assignment. i.e. hands-on experience, data processing, and summary of important aspects.

#### Repeat Examination:

#### (Recommended) Prerequisites:

Basic physical concepts, materials, electronic devices, fundamentals of Nanoelectronics.

The student should have (but it is not mandatory) taken classes in

- Nanoelectronics
- Nanotechnology

**Content:**

In this module, starting from fundamentals of nanofabrication and nanotechnology, concepts and requirements of nanosystems will be discussed. Numerous examples of nanosystems already existing today (logic gates, integrated memories, hard disks, ... ) will be presented and discussed. Characterization methods (optical, electrical, particle-based, magnetic) will be linked to structuring methods of nanotechnology, which are indispensable for the ultimate scaling of nanoobjects. Selected current research fields in nanoelectronics, nanomagnetism and optoelectronics, as well as in the application areas of logic, memory and sensing, will be used to exemplify the boundary conditions for (commercially) successful nanosystems.

In the part of the lecture, where the focus is on current research topics in micromagnetism, the students will get to know a research topic practically in parallel to lectures within the framework of a laboratory project. In small groups of max. 3 students, the characterization of e.g. ferromagnetic resonance effects in ferrimagnetic / ferromagnetic thin films using vector network analyzers and lock-in techniques will be directly experienced in the laboratory experiment and directly linked to what has been learned in the lectures.

**Intended Learning Outcomes:**

After completion of the module, students are able to evaluate nanodevices and their system integration. They are able to comprehensively review various different physical effects for their application in nanosystems. They know how to evaluate a physical effect in terms of scaling abilities to form a system. They are able to document and present the results of their experiments in form of a scientific report and graphs.

**Teaching and Learning Methods:**

The theoretical background to understand the operation of nanosystems will be provided in the lectures with traditional methods (power point presentations, discussion, questions in the lecture notes). Part of the module will be carried out in a hands-on lab. Small groups will work in a coordinated fashion towards the measurement and metrology of magnetic thin film devices.

**Media:**

The following types of media will be used:

- Presentation slides
- Lecture Notes
- Black board
- Hands-on lab

**Reading List:**

- Rainer Waser (Ed.), "Nanoelectronics and Information Technology" Advanced Electronic Materials and Novel Devices, Wiley-VCH, Third Edition, 2012.
- Sami Franssila, "Introduction to Microfabrication", John Wiley & Sons, 2010.
- J.M.D. Coey, Magnetism and Magnetic Materials, Cambridge University Press, 2009.
- Additional reading material and useful web sources will be provided to the students with the lecture notes / MOODLE course.

**Responsible for Module:**

Becherer, Markus; Prof. Dr.-Ing. habil.

**Courses (Type of course, Weekly hours per semester), Instructor:**

Nanosystems (Vorlesung, 4 SWS)

Becherer M [L], Becherer M ( Greil J )

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### EI7384: System-on-Chip Technologies | System-on-Chip Technologies [SoC1]

Version of module description: Gültig ab summerterm 2017

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 105	<b>Contact Hours:</b> 45

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The module exam is a written exam (75 min).

Students demonstrate that they have gained both fundamental and deeper understanding in various aspects of System on Chip Technologies and their analysis, from combinatorial logic to complete Embedded Systems. They have to answer the questions with self-formulated responses, checking boxes of multiple choice questions, sketch circuit or qualitative performance diagrams and do quantitative calculations. The allowed support material is constraint to a single sheet, individually prepared reminder notice.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Bachelor courses on semiconductor devices and digital circuits, basics in computer architecture

#### Content:

This course provides basics, current trends and challenges in the development of digital system-on-chip (SoC). We start with the main steps for building arbitrary CMOS-based combinatorial logic and sequential digital data processing and control circuitry (e.g. Finite State Machines) and explaining their role and significance in the scope of key system-on-chip components: microprocessors, memories and interconnects. The microarchitectural structure and building blocks of processor elements (RISC cores), on-/off-chip memory technology (SRAM, DRAM, Flash), bus and point-to-point interconnect standards (Processor Local Bus, Advanced Microcontroller Bus Architecture, FIFO) as well as the design of communications specific arithmetic blocks (adder, multipliers, shift and comparators) will be introduced and analyzed. Finally, we will introduce main implementation methods for SoCs, such as FPGA, standard cell and full custom

design, and discuss methods for low power design, which is vital for the development of SoCs in embedded systems.

**Intended Learning Outcomes:**

At the end of the module students are able to analyze and evaluate the structure and operation of systems-on-chip, including its main building blocks, e.g. processor, on-/off-chip memories, and interconnect, as well as implementation methods and techniques for low power consumption.

**Teaching and Learning Methods:**

Lecture material is accompanied by corresponding tutorials.

Students will analyze technical publications (as distributed during the course) like data-sheets as representation of building blocks and for usage in own developments of building blocks during the tutorials.

**Media:**

- Presentations
- Lecture notes
- Exercises with solutions as download

**Reading List:**

- J. Hennessy, "Computer Architecture. A Quantitative Approach", Elsevier
- J. Rabaey, "Digital Integrated Circuits", Prentice Hall
- N. Weste, K. Eshraghian, "Principles of CMOS VLSI Design", Addison Wesley

**Responsible for Module:**

Herkersdorf, Andreas; Prof. Dr.

**Courses (Type of course, Weekly hours per semester), Instructor:**

System-on-Chip Technologies (Vorlesung mit integrierten Übungen, 3 SWS)

Attal Z [L], Herkersdorf A, Wild T, Huang S, Stechele W

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Test and Evaluation Laboratory Course | Test- und Evaluierungspraktikum

### Module Description

#### CIT431013: Chip Design Test and Evaluation Laboratory Course | Chip Design Test and Evaluation Laboratory Course [CDTEL]

Version of module description: Gültig ab winterterm 2026/27

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 90	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

Achievement of the learning objectives is demonstrated by a project work which is supplemented by documentation of the results (approx. 3 pages per student) and a presentation. The project work includes the commissioning of a chip and the performance of measurements according to a catalog of requirements. The individual results are documented. The ability to assess and explain the results is demonstrated in the form of a group presentation lasting approx. 30 minutes (approx. 5 minutes per student followed by questions), whereby questions can also be asked regarding the individually documented results. The grade is based entirely on this oral examination.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Before taking this module, students should complete the Research Laboratory Physical Design of Integrated Analog and Mixed-Signal Circuits or the Research Laboratory Physical Design of Integrated Digital Circuits.

#### Content:

This internship is offered in the form of a block course and builds on the Digital Backend Design or Analog Backend Design research internship. A chip developed there or equivalent is put into operation by students. To this end, students work in small groups to develop the necessary control for testing a sub-circuit that they have usually developed themselves in a previous practical course; the specific functionality of the sub-circuit may vary; examples include AI accelerators, cryptographic algorithms, co-processors, or phase-locked loops. The students

carry out metrological investigations and characterizations for this subcircuit, e.g., with regard to power consumption or temporal behavior, compare the results achieved with previously defined specifications and thus determine the quality of the developed chip. The results are presented in the form of a seminar.

**Intended Learning Outcomes:**

After successfully completing this module, students will be able to

- Realise the commissioning of an Application Specific Integrate Circuit (ASIC),
- Independently evaluate the functionality of an integrated circuit, and
- Evaluate the quality of an integrated circuit with regard to typical criteria such as power consumption or time behavior by measurement.

**Teaching and Learning Methods:**

This practical course has the character of group-oriented project work in which students carry out experiments but also have to work out solutions independently. The objectives are discussed in an introductory event; in accompanying seminars and feedback sessions, students receive feedback on individual difficulties.

**Media:**

In the introductory course, slides and blackboard notes are used to convey content. Students also receive digital access to program code and materials for carrying out the internship tasks and individual feedback in discussions.

**Reading List:**

- Litovski, Vančo B. Lecture Notes in Analog Electronics: Testing and Diagnosis of Analog and Mixed-Signal Electronic Circuits. 1st ed. 2025. Springer Nature Singapore, 2025. <https://doi.org/10.1007/978-981-97-8257-4>.

-Bengtsson, Lars. Electrical Measurement Techniques: For the Physics Laboratory. 1st ed. 2024. Springer Nature Singapore, 2024. <https://doi.org/10.1007/978-981-99-8187-8>.

Students are informed about additional suitable literature in the introductory course.

**Responsible for Module:**

PD Dr.-Ing. habil. Michael Pehl

**Courses (Type of course, Weekly hours per semester), Instructor:**

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Pass Credit Requirement (doesn't count for the final grade) | Studienleistungen (gehen nicht in die Endnote ein)

### Research Internship | Forschungspraxis

#### Module Description

## CIT431014: Research Laboratory Functional Design of Integrated Digital Circuits | Research Laboratory Functional Design of Integrated Digital Circuits [FDDC]

Version of module description: Gültig ab summerterm 2026

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> summer semester
<b>Credits:*</b> 10	<b>Total Hours:</b> 300	<b>Self-study Hours:</b> 240	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The academic achievement is shown in form of a project work (in a group of around 5 people) in which students demonstrate that they can develop a suitable RTL description based on an algorithmic description and a given specifications and, from this, a netlist description of a digital circuit. In addition, functional tests for the design must be developed and successfully carried out. The design steps and the tests must be documented. The written documentation of the design and tests must be submitted at the end of the module and comprises approximately 5 pages per student, in which the individual contributions to the project are presented. Successful completion of the individual subtask must be demonstrated in order to pass the coursework.

The project work also includes a presentation in which the students demonstrate that they can present and discuss the progress and results of the project in a clear manner and in way showing their expertise (in groups, approx. 20 - 25 minutes or approx. 5 minutes per student with subsequent discussion).

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

HDL Chip Design Laboratory

## **Content:**

In this module, students work in groups to create an register transfer level (RTL) description of a circuit based on an algorithm and from that a gatelevel netlist of this circuit. As a starting point, the students receive a textual description of an algorithm from a current topic area (for example from the field of hardware security or hardware acceleration for artificial intelligence) as well as literature to familiarize themselves with the task. Depending on the relevant subject areas, students are also given specific objectives for the development of the hardware for these algorithms. Examples here could be the development of a design with the smallest possible surface area, the lowest possible power consumption or the lowest possible latency; objectives such as avoiding side-channel failure in circuits from the field of security can also be an objective.

Following the familiarization, the students first partition their design with regard to the division into hardware and software components and divide the complex design into manageable logical blocks, for example with the help of the Kactus 2 tool. For these blocks, the students develop an RTL description of the circuit. This is done using a hardware description language (VHDL, Verilog or SystemVerilog). In addition, students develop tests to ensure the functional correctness of their circuit and its sub-modules. These are developed in accordance with the Universal Verification Methodology (UVM), for example. Simulation tools from commercial providers such as Cadence, Siemens or Synopsys are used in the process of testing.

After successful testing, students synthesize their circuit into a gatelevel netlist with the help of a commercial design automation tool, such as those offered by Cadence or Synopsys, and use the corresponding tools from the same providers to prove that the circuit is functionally correct even after this step. The development or adaptation of scripts, e.g. in the language TCL, which is widely used in electronic design automation, is necessary for both steps. Students also check the synthesis reports of their circuit for compliance with specifications and optimize their circuit if necessary.

When synthesizing the RTL description, a so-called cell library is used, which may be subject to special confidentiality and licensing agreements in the case of commercial manufacturers and technologies used in today's industry. Students who wish to take advantage of the opportunity to have the developed chip manufactured after the second part of the practical course may have to sign a corresponding agreement. Students who do not wish to sign this agreement can alternatively use a cell library adapted for teaching or an open source alternative; the same learning outcomes are achieved; however, subsequent production cannot then be offered.

In addition to the technical aspects mentioned, students learn principles and techniques for project planning and project work (e.g. project structure planning, creation of requirements catalogs and specifications), as well as group work, such as the structural requirements for group work or the method of moderation.

## **Intended Learning Outcomes:**

After successfully completing this module, students will have acquired the following skills:

- They are able to develop a hardware description for a complex digital circuit starting from an abstract description and considering given specifications and apply the necessary steps to translate it into a description at netlist level.
- They are able to analyze the algorithmic description as well as their derived hardware description with regard to potential improvements and use the results of this analysis to improve their circuit.

- They are able to develop tests and can use them to check the functional correctness and compliance with the specifications for the circuit at RTL and netlist level.
- They understand the principles (e.g. methods of moderation) of group work and project planning (e.g. project structure planning, creation of requirements catalogs and specifications) and can apply these to design a project in the field of circuit design.
- They can clearly present the design and optimization strategies used in the process of logical design to a specialist audience.

**Teaching and Learning Methods:**

The basics for the lab are taught in approximately two introductory seminars. In particular, the work steps to be carried out, the specifications to be achieved and the design tools used are presented. In approximately three further seminars, content relating to group work and project planning is taught. The internship project is carried out independently in small groups of approx. 5 students in the scope of self-study in free time allocation. There is a regular exchange with a supervisor in the form of approx. weekly seminars and individual support and tutorials in the lab room (e.g. personal support in solving difficult problems in individual design); in this context, problems of the groups with the design and project organization are discussed and solved together.

**Media:**

Digital presentations and blackboard notes are used in the seminars. Students are also provided with documentation for the design tools used and the design tools themselves.

**Reading List:**

Suitable literature will be made available to students in the introductory course, depending on the project.

**Responsible for Module:**

PD Dr-Ing. habil. Michael Pehl

**Courses (Type of course, Weekly hours per semester), Instructor:**

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### CIT431015: Research Laboratory Functional Design of Integrated Analog and Mixed-Signal Circuits | Research Laboratory Functional Design of Integrated Analog and Mixed-Signal Circuits [FDAC]

Version of module description: Gültig ab summerterm 2026

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> summer semester
<b>Credits:*</b> 10	<b>Total Hours:</b> 300	<b>Self-study Hours:</b> 240	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The module is examined in the form of a project work (in a group of about 5 people) in which students demonstrate that they can develop the circuit diagram of an analog/mixed-signal circuit based on a given specification. They must also develop tests for the design and successfully carry them out according to their function. The individual design steps and the tests must be documented. The written documentation of the design and tests must be submitted at the end of the module and comprises approximately 5 pages per student, in which the individual contributions to the project are presented. Successful completion of the individual subtask must be demonstrated in order to pass the coursework.

The project work also includes a presentation in which the students demonstrate that they can present and discuss the project progress and results of the front-end design or the design and optimization strategies used in a clear and knowledgeable manner (in groups, approx. 20 - 25 minutes or approx. 5 minutes per student with subsequent discussion).

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Lab Analog RF Chip Design

#### Content:

In this module, students work in groups to develop an analog/mixed-signal circuit at transistor level based on a specification. The students realize a circuit from a typical subject area (examples can be a PLL, an ADC or a DC/DC converter). Depending on the specific topic, students implement specific objectives in the development of the hardware. Examples may include the development of a design with the smallest possible surface area or the lowest possible power consumption.

The circuit is first described at transistor level using a design tool such as those offered by Cadence or Synopsis. The transistor netlist of the circuit is developed and the transistors are suitably dimensioned. Among other things, methods of mathematical modeling of circuits are used to arrive at an initial transistor level description from the specifications; in addition, knowledge acquired in lectures is applied to carry out an initial dimensioning of the circuits. In addition, students develop tests in the form of simulations (here, for example, simulation methods such as transient analysis or periodic steady-state analysis must be suitably selected and stimuli specified) to ensure the functional correctness of their circuit. As part of the test, students check compliance with specifications and optimize their circuit if necessary.

So-called Process Design Kits (PDKs) are used in the development of the circuits, which may be subject to special confidentiality and licensing regulations for commercial manufacturers and technologies currently used in industry. Students who wish to take advantage of the opportunity to have the developed chip manufactured after the second part of the internship may have to sign a corresponding agreement. Students who do not wish to sign this agreement can alternatively use a cell library adapted for teaching or an open source alternative; however, it will probably not be possible to offer industrial production at a later date. The intended learning outcomes (see above) can be achieved in both cases, regardless of the tools used.

In addition to the technical aspects mentioned, the seminar teaches principles and techniques for project planning and project work (e.g. project structure planning, creation of requirements catalogs and specifications) as well as group work, such as the structural prerequisites for group work or the method of moderation.

### **Intended Learning Outcomes:**

After successfully completing this module, students will have acquired the following skills:

- They are able to develop the circuit diagram of a sophisticated analog/mixed-signal circuit at transistor level based on given specifications.
- They are able to analyze the developed circuit with regard to its technical improvement potential and use the results of this analysis to improve the circuit.
- They are able to develop tests in the form of simulations and can use these to check the functional correctness and compliance with the specifications for the circuit at transistor level.
- They can apply the principles of group work (e.g. moderation methods) and project planning (e.g. project structure planning, creation of requirements catalogs and specifications) to design a project in the field of circuit design.
- They can clearly present the design and optimization strategies used in the process of logical design to a specialist audience.

### **Teaching and Learning Methods:**

The basics for the lab are taught in approximately two introductory seminars. In particular, the work steps to be carried out, the specifications to be achieved and the design tools used are presented. In approximately three further seminars, content relating to group work and project planning is taught. The internship project is carried out independently in small groups of approx. 5 students in the scope of self-study in free time allocation. There is a regular exchange with a supervisor in the form of approx. weekly seminars and individual support and tutorials in the lab room (e.g. personal

support in solving difficult problems in individual design); in this context, problems of the groups with the design and project organization are discussed and solved together.

**Media:**

Digital presentations and blackboard notes are used in the seminars. Students are also provided with documentation for the design tools used and the design tools themselves.

**Reading List:**

Suitable literature will be made available to students in the introductory course, depending on the project.

**Responsible for Module:**

PD Dr.-Ing. habil. Michael Pehl

**Courses (Type of course, Weekly hours per semester), Instructor:**

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### CIT431017: Research Laboratory Physical Design of Integrated Digital Circuits | Research Laboratory Physical Design of Integrated Digital Circuits [PDDC]

Version of module description: Gültig ab winterterm 2026/27

<b>Module Level:</b>	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 90	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The academic achievement is shown in form of a project work (in a group of around 5 people) in which students demonstrate that they can develop a GDSII description of a circuit based on a netlist description of a digital circuit and specifications which, in addition to the given specifications, takes into account all design rules necessary for a successful tape-out. In addition, tests for the implemented design must be carried out successfully and the design steps and tests must be documented. The written documentation of the design and tests must be submitted at the end of the module and comprises approximately 5 pages per student, in which the individual contributions to the project on physical design are presented. Successful completion of the individual subtask must be demonstrated in order to pass the coursework.

The project work also includes a presentation in which the students demonstrate that they can present and discuss the progress and results of the project in a clear and informed manner (in groups, approx. 20 - 25 minutes or approx. 5 minutes per student with subsequent discussion).

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Research Laboratory Functional Design of Integrated Digital Circuits

#### Content:

The content of this module is the creation of a physical design from the gate netlist of a digital circuit. Current design methods and design tools (e.g. for automated placement and routing) are used, such as those provided by the commercial providers Cadence or Synopsis. Students develop the scripts required to carry out the design process (for example in the TCL scripting language commonly used in design automation) and work through the individual steps of

the physical design flow, which essentially consist of the following sub-steps: Floorplanning, Placement and Routing, Clock Tree Synthesis, Timing Closure, Power Optimization, Design for Manufacturability and Physical Verification and Signoff. Students come into contact with design rules (e.g., regarding placement and alignment of logic cells) for the technology used and learn to control the design process in such a way that these design rules are adhered to.

Manufacturer-specific standard cell libraries and process design kits (PDKs) are used for the steps required to create a chip suitable for production. For current industry-relevant technology nodes, one of which is also to be used in the planned chip manufacturing in the practical course, special license and non-disclosure agreements must be accepted for access to this data and must be signed by students. Students who do not wish to sign such agreements can alternatively work with a provided open source PDK or a PDK modified for teaching purposes, for which no signature is required. In this case, however, it will likely not be possible to produce the chip. The targeted learning objectives can be achieved in both cases and independent from the used PDK.

### **Intended Learning Outcomes:**

After successfully completing this practical course, students will have acquired the following skills:

- They are able to develop a tape-out-capable description of a complex digital circuit (GDSII) based on a netlist description and taking into account given specifications, applying technology-dependent design rules.
- They are able to check the functional correctness and compliance with the specifications of the developed hardware according to the physical design.
- You will be able to present the results of the back-end design steps clearly to a specialist audience and discuss them competently.

### **Teaching and Learning Methods:**

In this module, students working in groups are given the task of converting a netlist, which was developed by the same group in the “Research Laboratory Functional Design of Integrated Digital Circuits”, for example, into a description that can then be taped out. Typical specifications such as area or target frequency must be fulfilled. The students deal with a sub-area of a more complex circuit and consider the design rules for a given production technology for this sub-area. The students also develop tests to ensure the functionality of the circuit and compliance with the specifications after the back-end design.

As an introduction, the basics for the practical course are taught in approximately two seminars. In particular, the work steps to be carried out, the specifications to be achieved and the design tools used are presented. The practical course is carried out independently in small groups of approx. 5 students with free time allocation. Support is provided in the form of regular exchanges with a supervisor, in the form of weekly seminars or individual support and tutor sessions in the lab room (e.g., individual support for solving difficult problems in the student specific design); in this framework, problems of the groups with the design as well as with project organization will be discussed and jointly solved.

**Media:**

Digital presentations and blackboard notes are used in the seminars. Students are also provided with documentation for the design tools used and the design tools themselves.

**Reading List:**

Suitable literature will be made available to students in the introductory course, depending on the project.

**Responsible for Module:**

PD Dr.-Ing. habil. Michael Pehl

**Courses (Type of course, Weekly hours per semester), Instructor:**

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### CIT431018: Research Laboratory Physical Design of Integrated Analog and Mixed-Signal Circuits | Research Laboratory Physical Design of Integrated Analog and Mixed-Signal Circuits [PDAC]

Version of module description: Gültig ab winterterm 2025/26

<b>Module Level:</b>	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 5	<b>Total Hours:</b> 150	<b>Self-study Hours:</b> 90	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

The academic achievements of this module are demonstrated in form of a project work (in a group of about 5 people) in which the students demonstrate that they can develop a GDSII description of a circuit based on the circuit diagram of an analog/mixed-signal circuit and specifications, which, in addition to the given specifications, takes into account all design rules necessary for a successful tape-out. In addition, tests for the implemented design must be successfully carried out and the design steps and tests must be documented. The written documentation of the design and tests must be submitted at the end of the module and comprises approximately 5 pages per student, in which the individual contributions to the project are presented. Successful completion of the individual subtask must be demonstrated in order to pass the coursework.

The project work also includes a presentation in which the students demonstrate that they can present and discuss the progress and results of the project regarding physical circuit design in a clear and informed manner (in groups, approx. 20 - 25 minutes or approx. 5 minutes per student with subsequent discussion).

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

Research Laboratory Functional Design of Integrated Analog and Mixed-Signal Circuits

#### Content:

The content of this module is the creation of a physical design from the schematic of an analog/mixed-signal circuit. Current design methods and design tools (e.g., tools for place and route), such as those offered by the companies Cadence and Synopsis, are used. Students develop the scripts required to carry out the design process (for example in the TCL scripting language

commonly used in design automation) and work on the individual steps of the physical design flow, in particular floorplanning, analog placement and routing, physical verification and signoff. Students come into contact with design rules (e.g., regarding spacing of transistors) for the technology used and learn to control the design flow in such a way that the design rules are adhered to.

Manufacturer-specific process design kits (PDKs) are used for the steps required to create a chip suitable for production. For current industry-relevant technology nodes, one of which is also to be used in the planned chip production in the practical course, special license and non-disclosure agreements must be observed for access to this data, which must be signed by students. Students who do not wish to sign this agreement can alternatively work with a provided open source PDK or a PDK modified for teaching purposes, for which no signature is required. In this case, however, it will likely not be possible to produce the chip (in a fab). The targeted learning objectives can be achieved in both cases and independent from the used PDK.

### **Intended Learning Outcomes:**

After successfully completing this practical course, students will have acquired the following skills:

- They are able to develop a tape-out-capable description of a complex analog/mixed-signal circuit (GDSII) starting from a schematic and considering given specifications, applying technology-dependent design rules.
- They are able to check the functional correctness and compliance with the specifications of the developed hardware according to the physical design.
- You will be able to present the results of the back-end design steps clearly to a specialist audience and discuss them competently.

### **Teaching and Learning Methods:**

In this module, students work in groups to develop from the schematic of a circuit that was designed by the same group in the “Research Laboratory Functional Design of Integrated Analog and Mixed-Signal Circuits”, for example, into a description that can then be taped out. Typical specifications such as area or power consumption must be adhered to. The students deal with a sub-area of a more complex circuit and consider the design rules for a given production technology for this sub-area. The students also develop tests to ensure the functionality of the circuit and compliance with the specifications after the back-end design.

As an introduction, the basics for the practical course are taught in approximately two seminars. In particular, the work steps to be carried out, the specifications to be achieved and the design tools used are presented. The practical course is carried out independently in small groups of approx. 5 students with free time allocation. Support is provided in the form of regular exchanges with a supervisor, in the form of weakly seminars or individual support and tutor sessions in the lab room (e.g., individual support for solving difficult problems in the student specific design); in this framework, problems of the groups with the design as well as with project organization will be discussed and jointly solved.

### **Media:**

Digital presentations and blackboard notes are used in the seminars. Students are also provided with documentation for the design tools used and the design tools themselves.

**Reading List:**

Suitable literature will be made available to students in the introductory course, depending on the project.

**Responsible for Module:**

PD Dr.-Ing. habil. Michael Pehl

**Courses (Type of course, Weekly hours per semester), Instructor:**

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Interdisciplinary Modules | Außerfachliche Ergänzung

### Module Description

## IN2021: Computer Aided Medical Procedures | Informatikanwendungen in der Medizin

Version of module description: Gültig ab summerterm 2024

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> winter semester
<b>Credits:*</b> 6	<b>Total Hours:</b> 180	<b>Self-study Hours:</b> 120	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

### Description of Examination Method:

Type of Assessment: exam

The exam takes the form of a written test. The duration is 90 minutes and no material is allowed (closed book). Questions allow to assess whether the student is able to understand fundamentals, differences and application areas of medical imaging modalities as well as methods for medical image processing and computer aided surgery.

Participants who successfully complete voluntary small case studies receive a grade bonus of 0,3 on their exam grade. The grade bonus is only applied to passed examinations (grades including 1,3 to 4,0). The case studies are used to check whether participants are independently able to select an appropriate imaging modality or algorithm for a specific application.

### Repeat Examination:

End of Semester

### (Recommended) Prerequisites:

Bachelor in informatics or another scientific or technological course of studies

### Content:

The module IN2021 is concerned with topics such as:

- Overview
- ++ Computer aided medical procedures
- ++ History of radiology and surgical procedures
- Medical Imaging Modalities

- ++ X-ray
- ++ Computed tomography
- ++ Angiography
- ++ Magnetic resonance imaging
- ++ Ultrasound
- ++ Positron emission tomography
- ++ Optical imaging
- Computer Aided Systems for Diagnosis, Treatment, Surgery, and Follow-up
- ++ Image segmentation
- ++ Rigid and deformable image registration
- ++ Tracking systems
- ++ Visualization and augmented reality

These topics are augmented by invited talks of clinical or industrial experts.

**Intended Learning Outcomes:**

Upon successful completion of the module participants are able to understand and assess fundamental physical principles of medical imaging techniques as well as the fundamentals of algorithms for medical image processing and computer aided surgery.

Moreover, participants are able to identify problems in the area of diagnosis and therapy as well as to develop corresponding solution strategies based on the methods covered in the areas image processing, navigation and visualization.

**Teaching and Learning Methods:**

Lecture, tutorial, problems for individual study. Guest lectures will be held by experts from local hospitals and med-tech companies to ensure that the covered topics are relevant for clinical practice. The assignments are provided on a weekly basis via the teaching portal. They are discussed in the next tutorial class, and a solution is presented. Work on the assignments and participation in the tutorial class are voluntary. They serve as a means for students to deepen and test their acquired knowledge – as a self-monitoring aid to prepare for the written exam.

**Media:**

Slide show, blackboard

**Reading List:**

Terry M. Peters, Kevin Cleary: Image-Guided Interventions: Technology and Applications. Springer, 1st edition 2008

Terry M. Peters: Image-guided surgery: From X-rays to Virtual Reality. Comput Methods Biomech Biomed Engin, 4(1):27-57, 2000

**Responsible for Module:**

Navab, Nassir; Prof. Ph.D.

**Courses (Type of course, Weekly hours per semester), Instructor:**

Informatikanwendungen in der Medizin (IN2021) (Vorlesung, 4 SWS)

Navab N [L], Navab N, Eck U, Faghihroohi S, Tomczak A

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### SOT86701: EuroTeQ Collider. Enhancing Connections for Sustainable Futures (MSc) | EuroTeQ Collider. Enhancing Connections for Sustainable Futures (MSc)

Version of module description: Gültig ab summerterm 2024

<b>Module Level:</b> Master	<b>Language:</b> English	<b>Duration:</b> one semester	<b>Frequency:</b> summer semester
<b>Credits:*</b> 6	<b>Total Hours:</b> 180	<b>Self-study Hours:</b> 120	<b>Contact Hours:</b> 60

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

During this module, students must complete following tasks: producing a presentation that provides information on the project concept development and implementation, as well as a final report, charting the progress of their work/research over time. These assessments will evaluate a) the success of the project and b) the learning success of the students in oral and written form. Students will be graded based on the active participation in a group project (20%), a final presentation of project results (60%) and a final project report (20%). These examination requirements will assess the success of the project, but also examine the learning success of the students in oral and written form.

#### Repeat Examination:

Next semester

#### (Recommended) Prerequisites:

This module is aimed at all students enrolled in a Bachelor or Master program at the TUM; it is thus designed as an interdisciplinary venue which brings together a range of scientific perspectives. No specific prior knowledge is required; however, its project-based character requires high levels of intrinsic motivation and the willingness to actively participate in a project. Please register for this course via TUM Online. If you have any questions or problems to register, please send an email to [euroteq@ja.tum.de](mailto:euroteq@ja.tum.de)

#### Content:

"Enhancing Connections for Sustainable Futures" aims to promote an integrated approach based on three main areas: People, Nature, and Technology. In the "People" domain, the focus is on empowering and enabling communities. This involves connecting people's needs and aspirations through technology, including digital solutions, in various areas such as wellbeing,

health, culture, etc. In the "Nature" realm, the call concentrates on the conscious use of nature and the consideration of its resources. This includes examining interactions in ecosystems, safeguarding biodiversity and nature conservation, as well as utilizing renewable energies. Within the "Technology" sphere, the emphasis is on establishing efficient connections through technology, both digital and physical. This encompasses various fields such as information technology, logistics, transportation, manufacturing, communication, etc. Overall, the call aims to promote sustainable connections that enable meeting human needs, protecting the environment, and leveraging innovative technologies to achieve these goals.

The Technical University of Munich (TUM) joint forces within eight leading universities of science, technology and business to foster the European spirit in a EuroTeQ format to promote innovative engineering education across Europe. Together, we have created the first EuroTeQ Collider in 2022. Now, the journey goes into the second round. The Collider is an innovative learning format with the aim of bringing students together with vocational trainees and professionals to tackle challenges. The theme for the period 2024-2026 is "Enhancing connections for sustainable Futures". The goal is to connect participants with different profiles and personalities to boost creativity, innovation, shared understanding, enabling participants to imagine new approaches and design disruptive solutions.

The module is a seminar that gives students the opportunity to apply their knowledge on topics related to the theme "Enhancing connections for sustainable Futures". Within this overarching theme, we are offering challenges on three different topic-domains, namely:

- People – e.g., empowering and enabling communities, connecting people's needs and aspirations through technology (including digital solutions) in different areas such as wellbeing, health, culture, etc.
- Nature – e.g., on the conscious use of nature, taking into account environmental resources and the relationship of organisms to the environment: interactions in the ecosystem, safeguarding biodiversity and nature conservation, use of renewable energies, etc.
- Technology – e.g., efficient connections through technology, both digital and physical, in various areas such as information technology, logistics, transportation, manufacturing, communication, etc.

Within every topic domain, interdisciplinary (and international) teams of students, vocational trainees and professional learners are formed to develop solutions towards a desirable future, test and validate tools and create prototypes of their solutions. A selection of the best projects will be presented in a major high-level event, the EuroTeQaThon.

### **Intended Learning Outcomes:**

After completion, all EuroTeQ Collider participants will be able to:

- Select and apply appropriate design, engineering and business approaches and tools to create an innovative and science-based solution to a real-life challenge.
- Develop a profound interpretation of a complex, real-life problem and its context using a system-thinking approach, considering multiple perspectives.

- Develop a problem-driven, creative, and integrative design, demonstrated by a concrete prototype that balances desirability, feasibility, and viability.
- Use disciplinary knowledge and expertise in an inter-disciplinary team to develop an innovative and scientifically sound solution in a European context.
- Communicate your ideas, at different levels of elaboration, via several mediums in an international context to a diverse set of stakeholders.
- Define and regularly reflect on personal and team development.

### **Teaching and Learning Methods:**

A range of teaching & learning techniques will be applied:

- (pre-recorded) videos and online presentations, with podcasts and interviews, Q&A Sessions with experts
- This module is focusing on service-learning and project-based learning
- After a set of introductory sessions which provide input on the core topics but also project management, students will work on their projects in groups. Progress will be determined through project presentations during the semester, continuous feedback from the instructors, as well as peer-to-peer feedback.
- Presentational skills will be further facilitated through the requirement to present the results
- As students and professionals will work together in a joint effort, all participants will not only improve their technical skills but also enhance their soft skills such as team spirit, flexibility to work in multicultural environments, and design thinking, which are also very important in professional life.

### **Media:**

### **Reading List:**

### **Responsible for Module:**

Wester, Angela; M.A.

### **Courses (Type of course, Weekly hours per semester), Instructor:**

(SOT82701, SOT86701) EuroTeQ Collider. Enhance Connections for Sustainable Futures (Seminar, 4 SWS)

Wester A ( Finger P, Lehmann D, Schmid H ), Baumer D, Lau K, Miller N, Onyango F, Rufino M, Wang Y, Zhang Y

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

## Module Description

### SZ0337: German as a Foreign Language A1.1 | Deutsch als Fremdsprache A1.1

Version of module description: Gültig ab summerterm 2022

<b>Module Level:</b> Bachelor/Master	<b>Language:</b> Language taught	<b>Duration:</b> one semester	<b>Frequency:</b> winter/summer semester
<b>Credits:*</b> 4	<b>Total Hours:</b> 135	<b>Self-study Hours:</b> 90	<b>Contact Hours:</b> 45

Number of credits may vary according to degree program. Please see Transcript of Records.

#### Description of Examination Method:

Performance, testing the learning outcomes specified in the module description, is examined by a cumulative portfolio of competence and action-oriented tasks. Aids are permitted.

The examination performances are designed in their entirety to test the use of vocabulary and grammar, reading and/or listening comprehension, and free text production.

Oral communication skills will be tested via the use of appropriate idioms in written dialogue examples and/or in the form of an audio/video file. For this purpose, we observe the Basic Data Protection Regulation (DSGVO, Art. 12 -21).

#### Repeat Examination:

#### (Recommended) Prerequisites:

none

#### Content:

This module teaches basic knowledge of German as a Foreign Language, taking into account intercultural and cultural aspects of the country, which will enable students to find their way around despite their limited knowledge of the language, e.g. when shopping, in restaurants, on public transport, etc.

They will learn/practice basic vocabulary on topics such as family, work, leisure and food, ask and answer simple personal/family questions, understand and use numbers, prices and times and report everyday activities in simple structured main sentences in the present tense, using verbs, nouns, personal pronouns, possessive articles and negation forms.

Students practice teamwork skills by collaborating on tasks in multinational groups.

**Intended Learning Outcomes:**

The module is oriented towards level A1 of the CEFR. After completing this module, students will be able to use everyday expressions and very simple sentences aimed at meeting specific needs of everyday life: They can introduce themselves and others and ask other people questions about themselves and give answers to questions of this kind. They can describe daily routines in basic structures and give basic information about themselves in writing. They can communicate their needs if interlocutors speak clearly and slowly and are supportive. Students learn how to organize their own learning process of the foreign language independently and effectively.

**Teaching and Learning Methods:**

The module consists of a seminar in which students study the learning content with targeted listening, reading, writing and speaking exercises. The communicative and action-oriented approach is implemented by combining these exercises in individual, partner and group exercises. Online material for controlled self-study of basic grammatical phenomena and communication patterns is provided to deepen and intensify the content taught during the course. Voluntary homework (for preparation and revision) consolidates what has been learned.

**Media:**

Textbook, multimedia-supported teaching and learning material, also online

**Reading List:**

Textbook: will be announced in the course

**Responsible for Module:**

Christina Thunstedt

**Courses (Type of course, Weekly hours per semester), Instructor:**

Deutsch als Fremdsprache A1.1 (Seminar, 3 SWS)

Bakker S, Burmasova S, Endraß E, Grgic T, Hanke C, Huber D, Keza I, Koch H, Kraut-Schindlbeck S, Lechle K, Pinskaia I, Pletschacher T, Schmidt-Bender S, Selent D, von Caprivi Caprara de Montecucculi A, von Egloffstein A, Witzig B

Blockkurs Deutsch als Fremdsprache A1.1 (Seminar, 3 SWS)

Comparato G, Kretschmann A, Schippers M, Schlüter J, von Egloffstein A, Zerfass A

Deutsch als Fremdsprache A1.1 - EuroTeq Programm (Seminar, 3 SWS)

Lechle K

For further information in this module, please click [campus.tum.de](https://campus.tum.de) or [here](#).

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